COE211: Digital Logic Design

CH7 part 2:

Programmable Logic

Programmable Logic

- programmable logic can be programmed to perform specified logic functions
  - This can be done by the manufacturer or by the user.
- Advantage
  - designs can be readily changed without rewiring or replacing components

- programmable logic:

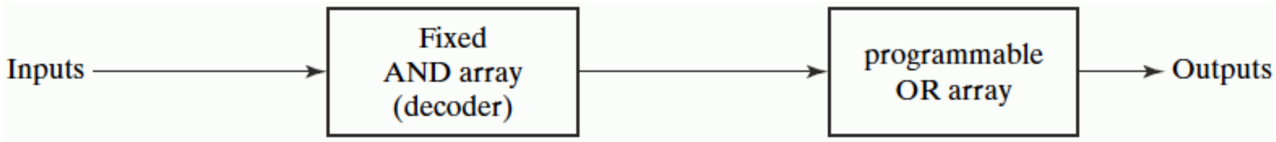
1. programmable logic Devices (PLD)
   - Combinational programmable logic
     - PLA
     - PAL
   - Sequential programmable logic
     - SPLD
     - CPLD
2. FPGAs

Combinational Programmable Logic Devices (PLDs)

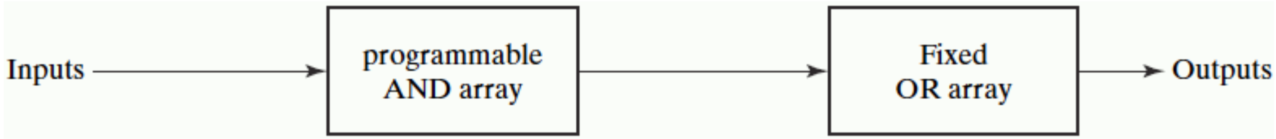
- "Generic" chip customized by designer
- Programming information used
- Programmable / Reprogrammable
  - Program once, then use it in circuit
  - Program and use, then erase, program and use
- Three types
  - Read Only Memory (ROM)
  - Programmable Logic Array (PLA)
  - Programmable Array Logic (PAL)

Programmable Logic Devices (PLDs)

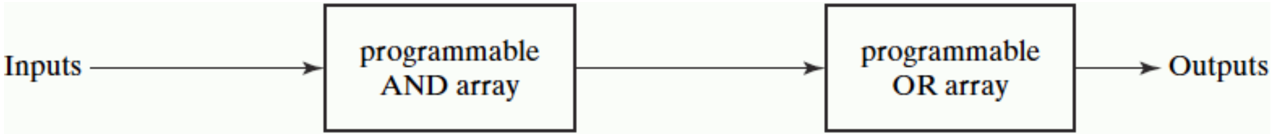
- Combinational Programmable Logic Device (PLD)
  - Convenient method for implementing combinatorial logic
  - Regular structure of AND-OR array
- Three possible implementations:
  - Programmable ROM (PROM)



  - Programmable Array Logic (PAL)

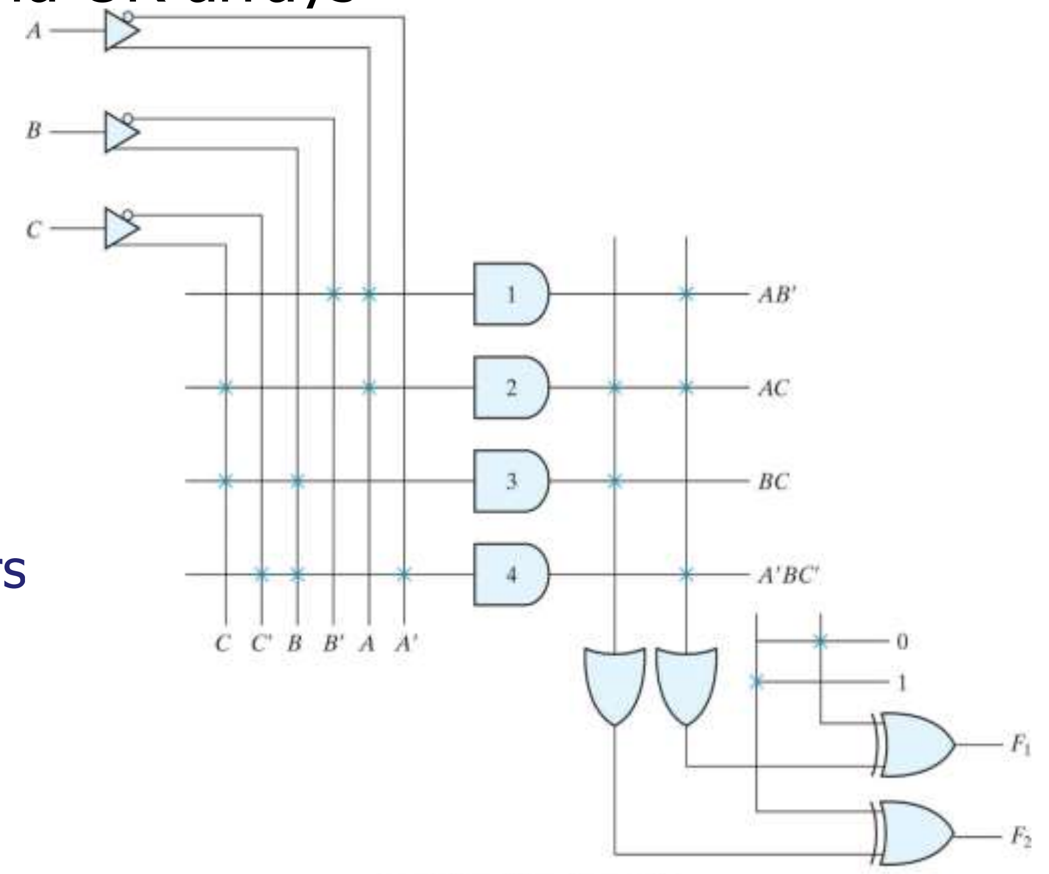


  - Programmable Logic Array (PLA)



Programmable Logic Array (PLA)

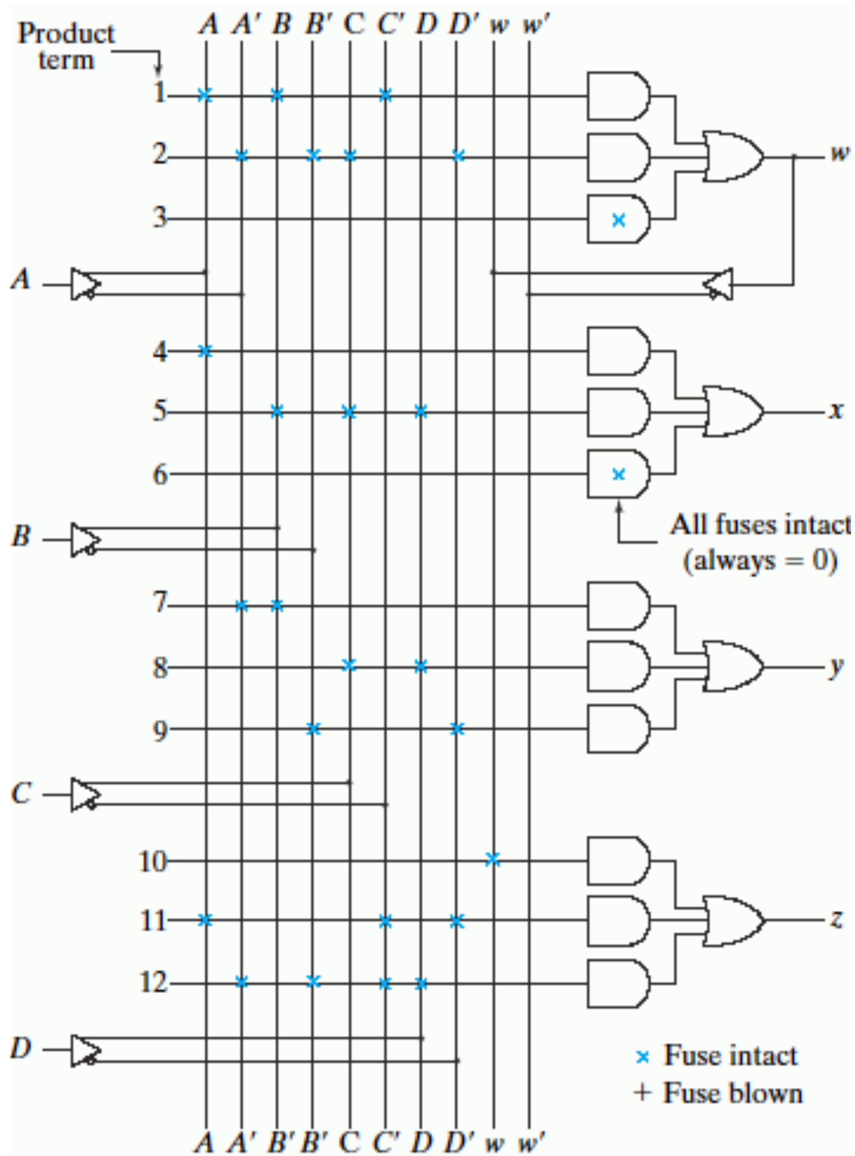
- Programmable AND and OR arrays
- AND array
  - generates products
- OR array
  - Generates sum of products
- Output XOR
  - Programmable inverters
- What is the function of this PLA?
  - F1 = AB′ + AC + A′BC′
  - F2 = (AC + BC)′



Programmable Array Logic (PAL)

- Programmable AND array and fixed OR array
- "Section" of PLA
  - Three-wide AND-OR array
  - AND generates product term "programmable"
  - OR generates sum "fixed"

  Three-wide (means 3-ANDs)
- Additional feedback
  - Output w is fed back to add new term
- Limitations?
  - Only three wide AND-OR
  - Not all functions may fit



PAL Example

- Implement
- F1(x,y,z)

  $=\Sigma\ (0,3,5,6)$

  $= x'y'z' + x'yz$

  $+xy'z + xyz'$

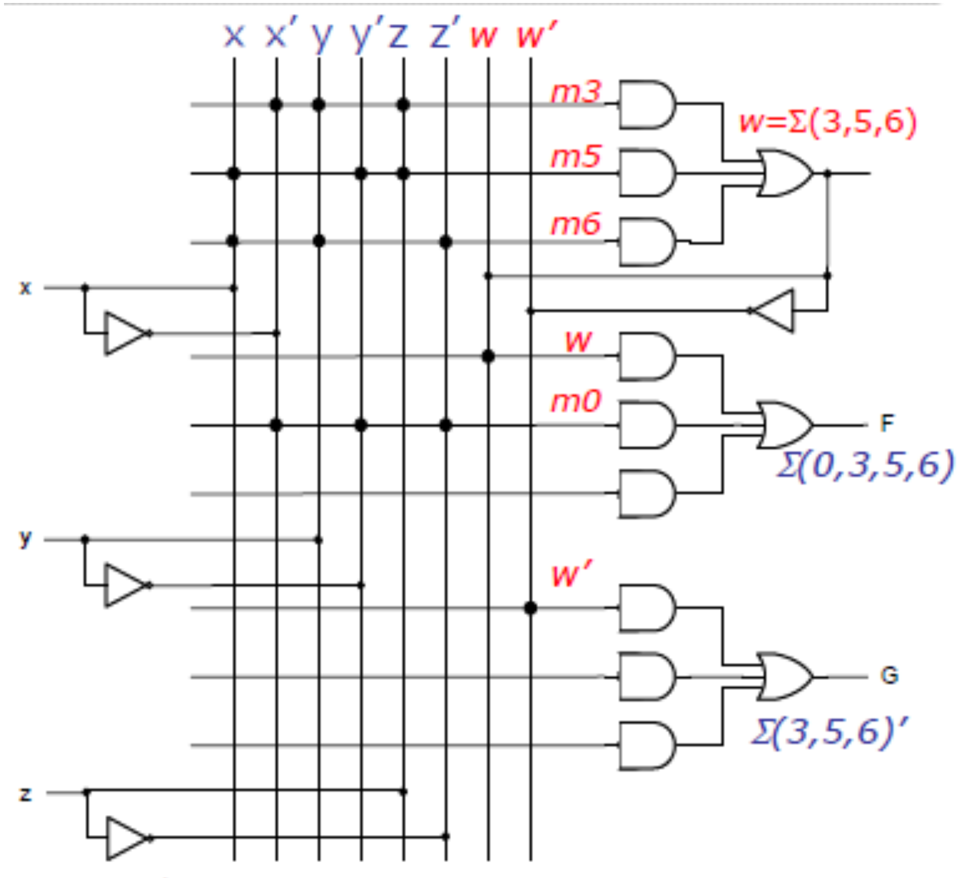
- F2(x,y,z)

  $= \Sigma(0,1,2,4,7)$

  $= \Sigma(3,5,6)'$

  $= x'y'z' + x'y'z$

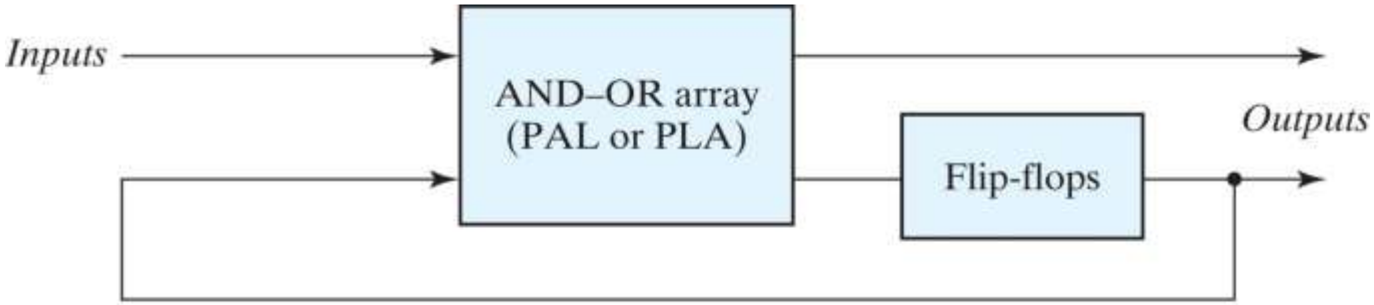
  $+x'yz' + xy'z' + xyz$



Sequential Programmable Devices

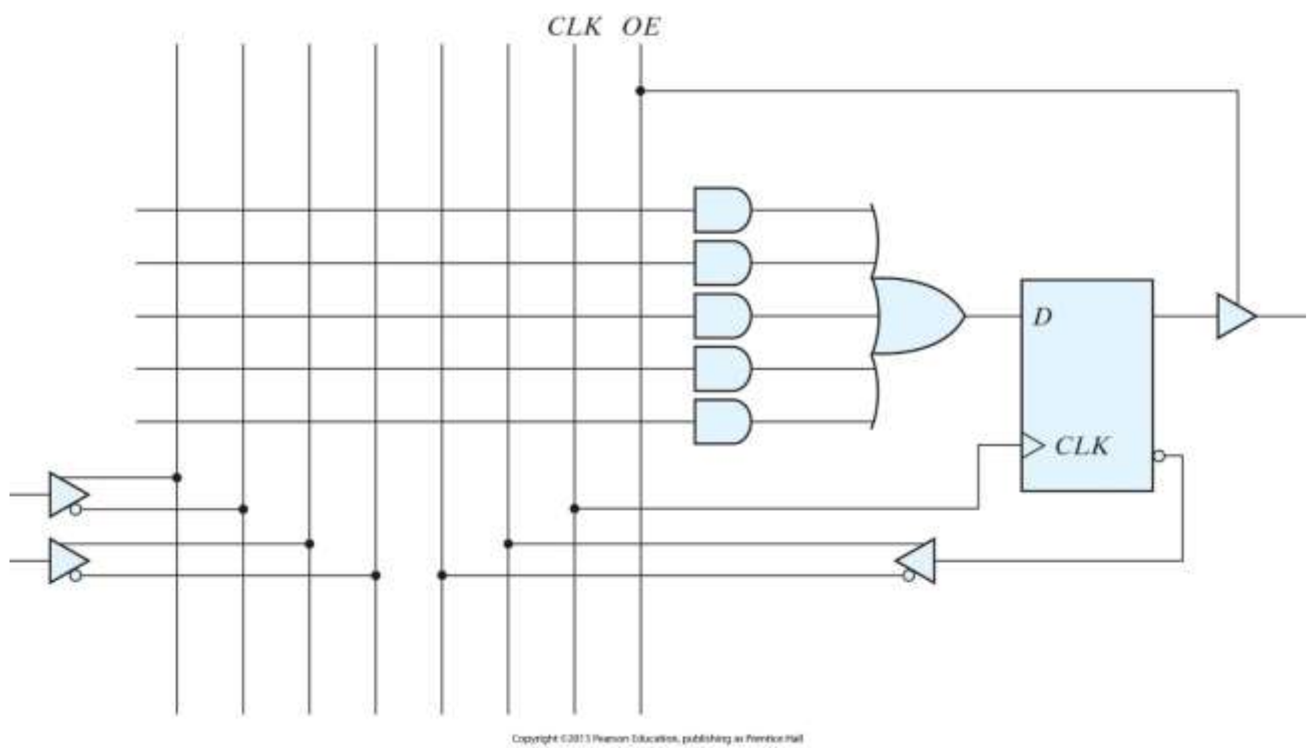
- PLDs convenient for combinatorial circuits

- Sequential programmable devices:
  - Sequential (Simple) programmable logic device (SPLD)
  - Complex programmable logic device (CPLD)



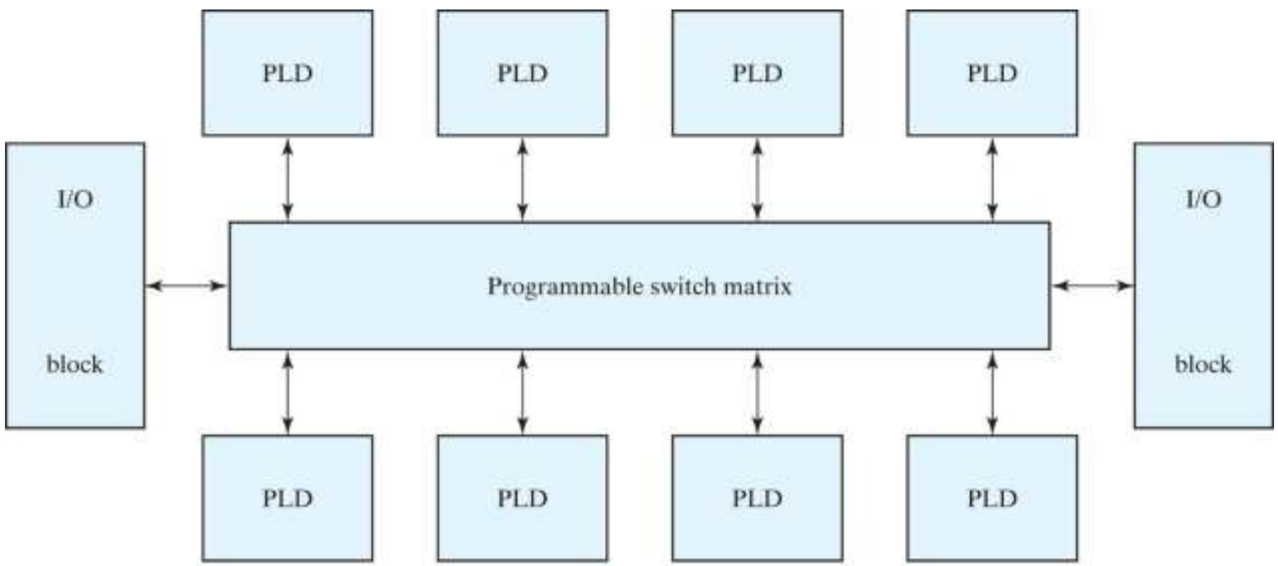
Sequential Programmable Logic Device

- SPLDs are mode from macrocells
  - Contains sum-of-product combinatorial logic (PAL)
  - Contains flip-flop (D-type)
- Macrocell:
  - Typically 8-10 per IC package



Complex Programmable Logic Device

- CPLDs for larger circuits
  - Combine multiple SPLDs
  - Switch matrix connects SPLDs
  - I/O block with tristate I/O
- Details are vendor-specific
  - Altera (CPLD)

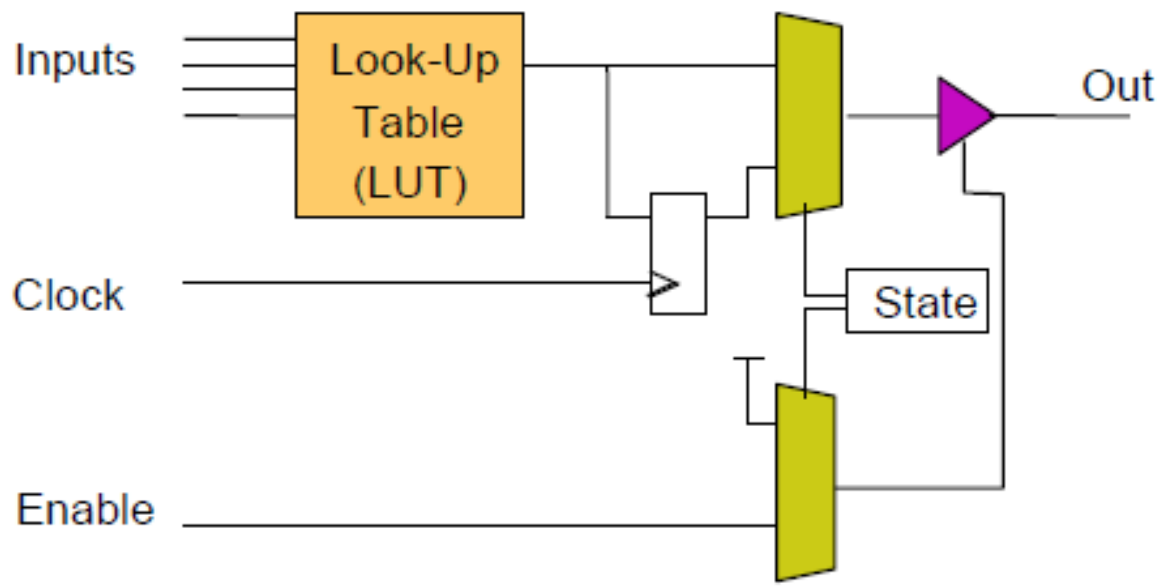


Field Programmable Gate Arrays

- Gate Array (VLSI Design)
  - An array of programmable logic function blocks
  - Gate array is manufactured ahead of time (prefabricated)
  - Customer programs (configures) the gate array
    - provides logic functions and interconnections
- Field Programmable Gate Array (FPGA)
  - An array of identical, programmable logic function blocks
    - Each block has a fixed number of inputs (k)
    - Each block is able to implement an arbitrary logic function
  - Customer programs FPGA after manufacturing, “in field”
    - Re-programmable
  - Easier to debug and cheaper in smaller quantity than ASIC (**application-specific integrated circuit**)
- An alternative to ASIC

Logic Element

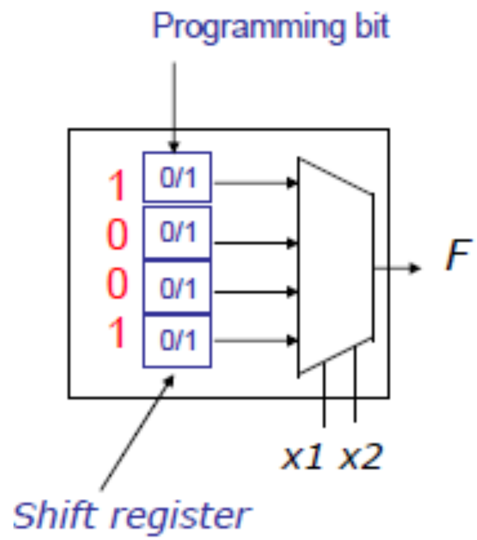
- Logic Element
  - the basic programmable element of FPGA
  - Contains LUT



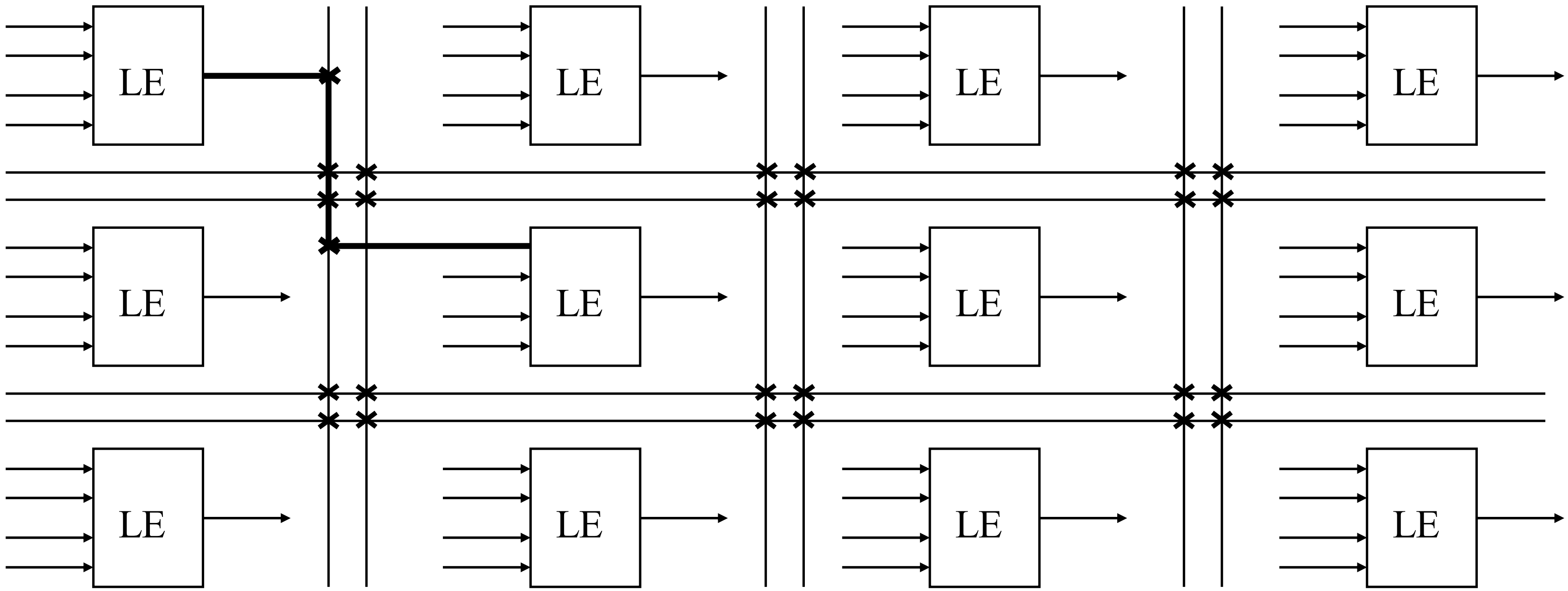
Look-up Table based FPGA

- Look-up Table (LUT)
  - Truth table implemented in hardware
  - Can implement arbitrary function with fixed number of inputs (typically 4-5) by programming the storage bits (customizing the truth table)
  - Example: 2-input LUT
  - F = x1′x2′ + x1x2

x1	x2	F
0	0	1
0	1	0
1	0	0
1	1	1



FPGA Architecture



- Each programmable logic element outputs one data bit.
- Interconnects are programmable between elements.
- Interconnect tracks grouped into channels.