Taibah University
College of Computer Science and Engineering
Department of Computer Science

Form A

Assignment – 1st Semester (2022/2023)

COE211 - Digital Logic Design

Submission deadline: Sunday: 06/11/2022 **Total: 5** Marks

Student Name: **Student No.:** **Section:**

Instructions to students:

1. **For solving this assignment, use your own words. Copying from any source (including web pages and books) or among students will be considered PLAGIARISM (i.e. dishonesty). This is a serious misconduct that causes a serious academic penalty, including zero marks for this assignment.**
2. **Any submission after the deadline will not be accepted.**

For instructors:

CLO	Questions	Assigned marks	Awarded marks
1.1	1	1	
1.2	2	1	
2.1	3	1	
2.4	4	1	
	5	1	
Total		**5**	

1) Using 2's complement, compute $(7)_{10} - (11)_{10}$ **(1 Mark)**

2) Simplify the following Boolean function using K-map. Draw the logic diagram for the simplified function. **(1 Mark)**

$$F = A'BCD' + B'CD + BC'D' + ACD' + A'B'C + B'C'D'$$

3) **Design a combinational logic circuit that detects even inputs which are in the range from 0 to 7. (1 Mark)**

4) **The contents of a four-bit register is initially 1001. The register is shifted five times to the right with the serial input being 01100110. What is the content of the register after each shift? (1 Mark)**

5) The memory unit that follow are specified by the number of words times the number of bits per word. How many address lines and input–output data lines are needed in each case? (1 Mark)

a) $16G \times 64$

b) $32M \times 8$