TAIBAH UNIVERSITY

College of Computer Science and Engineering

Computer Engineering Department

COE 211
Digital Logic Design

Prepared by
Dr. Aly El-SEMARY Dr. Omar TAYAN

Student Lab Manual

COE Version

Student Name: .....

Student ID: .....

Section: ..... **Group:** .....

Session (Fall / Spring / Summer): .....

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Acknowledgements

This lab guide has been primarily developed using a series of labs and material from the Lab-Volt courseware materials.
We are, also, grateful to Eng. Ibrahim Al-Haddadi and Dr. Amar Arbaoui for their support during the preparation of this student lab guide document.
We would also like to thank the head of the department Dr Mohamed Al-Saeidy for his support, guidance, and assistance in the final preparation of this student lab guide.

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	Assessment Criteria		Grade	CLOs	Excel file ID
COE211 Logic Design	Lab	Participation	5%	5.1,3.3,2.1,2.2,2.3,2.4	LP:5:5.1%3.3%2.1%2.2%2.3%2.4
		Lab Reports	10%	4.1, 4.2, 2.1, 2.2	LR:10:4.1%4.2%2.1%2.2
		Final Exam (Labs)	5%	4.2,4.3,2.1,2.2,2.3, 2.4	LabEx:5:4.2%4.3%2.1%2.2%2.3%2.4

LABORATORY SAFETY GUIDELINES

A. General Laboratory Safety Rules

1. Personal Safety

- Be familiar with the electrical and fire hazards associated with your workplace.
- Be as careful about the safety of others as for yourself. Think before you act.
- Be tidy and systematic.
- Avoid bulky, loose or trailing clothes. Avoid long loose hair.
- No one can enter in the lab area bare foot due to increased risk of electric shock.
- Remove metal bracelets, rings or watchstraps when working in the laboratories.
- Avoid working with wet hands and clothing.

2. Food, Beverages and Smoking

- Due to the increased risk of electric shock, no drinking of beverages, consumption, or storage of any kind of food is allowed in the laboratory.
- Smoking is prohibited in all laboratories in all timings.

3. Soldering

- No one can do soldering in any of the computer engineering laboratories except the graduation project design laboratory.
- Anyone doing soldering in the graduation project design laboratory must wear appropriate apparel, socks, gloves, covered shoes and safety goggles to prevent the possibility of severe burns resulting from the splashing or dripping of hot liquefied solder into the face and eyes or on to the exposed skin on the chest, hands, legs, and feet.
- Students who are not so properly attired for these tasks will NOT be allowed to perform any type of soldering in the graduation project design laboratory.

4. Laboratory Operating Hours

- Students are never allowed to work alone in any lab area other than scheduled laboratory operating hours unless either a Lab T/A or Course Instructor is present inside that lab area.
- The laboratory operating hours for students are posted on the entrance doorway and on the notice board of computer engineering department.

5. Power Supply Related Safety

- Voltages above **50-VAC** or **120-VDC** are always dangerous.
- Extra precautions should be considered as voltage levels are increased.
- Never make any changes to circuits or mechanical layout without first isolating the circuit by switching off and removing connections to power supplies.

6. Laboratory Equipment

- Lab equipment may not be removed from the Computer Engineering lab areas without the permission of the Laboratory Supervisors.
- Laboratory bench equipment (except for some lab bench computers) must be turned off before closing down the lab area for the day.
- Never open (remove cover) of any equipment in the laboratories.
- Never "jump," disable, bypass or otherwise disengage any safety device or feature of any equipment in the laboratories.
- Laboratories shall be locked when unoccupied.

7. Waste Management Safety

- Know the correct handling, storage and disposal procedures for batteries, cell, capacitors, inductors, and other high energy-storage devices.

8. Equipment Safety

- Before equipment is energized ensure, circuit connections and layout have been checked by a Teaching Assistant (TA) and all colleagues in your group has given their consent.
- Experiments left unattended should be isolated from the power supplies. If for a special reason, it must be left on, a barrier and a warning notice are required.
- Equipment found to be faulty in any way should be reported to the lab supervisor and taken out of service until inspected and declared safe.

9. Equipment Accessories

- Use extension cords only when necessary and only on a temporary basis.
- Request new outlets if your work requires equipment in an area without an outlet.
- Discard damaged cords, cords that become hot, or cords with exposed wiring.

B. Electrical and Fire Emergency Responses

1. Police, Fire or Medical Emergency

- Use the telephone located in the laboratory area and press **0-996** to notify police, fire, and ambulance for emergency help.
- Everyone present in the laboratory area shall be familiar with the locations and operation of safety and emergency equipment, including but not limited to, fire extinguishers, first aid kits, emergency power off system, fire alarm pull stations, and emergency telephones.

2. Electric Shock

- When someone suffers serious electrical shock, he may be knocked unconscious.
- If the victim is still in contact with electrical current, immediately turn off the electrical power source.
- If you cannot disconnect the power source, depress the Emergency Power Off switch.
- Do not touch a victim that is still in contact with a live power source; you could be electrocuted! Have someone call for emergency medical assistance immediately. Administer first-aid, as appropriate.

3. Electrical Fire

- If an electrical fire occurs, try to disconnect the electrical power source, if possible.
- If the fire is small and you are not in immediate danger; and if you have been properly trained in fighting fires, use the correct type of fire extinguisher to extinguish the fire.
- When in doubt, push in the Emergency Power Off button.
- **NEVER use water to extinguish an electrical fire**.

4. Emergency Power Off

- Every lab is equipped with an Emergency Power off System.
- When this switch is depressed, electrical power to the lab will shut off, except for lights.
- Only authorized personnel are permitted to reset power once the Emergency Power Off system has been engaged.

5. Building Evacuation in Emergency

- Everyone present in the laboratory should be familiar to emergency exits & way out plans.
- Use the nearest exit doorway from lab area closest to the stairwell to exit the building.
- Follow the Emergency Exit Signs posted in the hallways. Do not use elevators.
- Lab Teaching Assistants (T/As) or Instructor shall make sure all persons are out of the laboratory area and follow the directions posted at each doorway to the laboratory area.

The above general laboratory safety rules are designed to safeguard you and your co-workers, fellow students and colleagues and are a minimum requirement for individuals working in the computer engineering laboratories at Taibah University. Specialized training and rules may apply depending on type and scope of activities involved.

Lab 1A: Circuit Block Familiarization

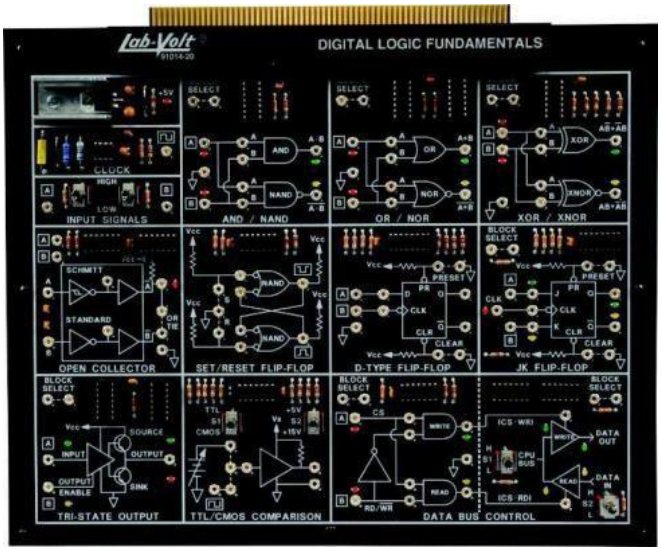
- **OBJECTIVE**

When you have completed this exercise, you will be able to locate and identify the circuit blocks and components on the DIGITAL LOGIC FUNDAMENTALS circuit board. You will verify your results by identifying logic circuits and making logic level measurements with a voltmeter and an oscilloscope.

- **Requirements**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - Personal Computer or Laptop.
  - A multimeter
  - An oscilloscope

- **DISCUSSION**

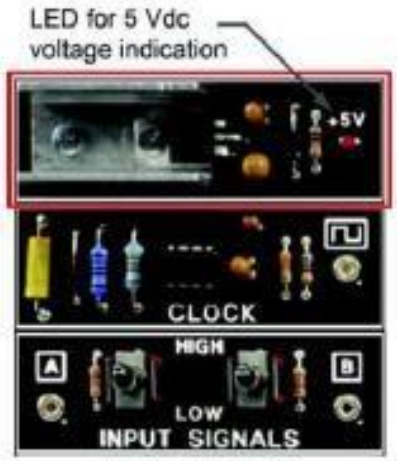
The DIGITAL LOGIC FUNDAMENTALS circuit board provides examples of logic circuits. There are thirteen circuit blocks on the DIGITAL LOGIC FUNDAMENTALS circuit board connected to your base unit.



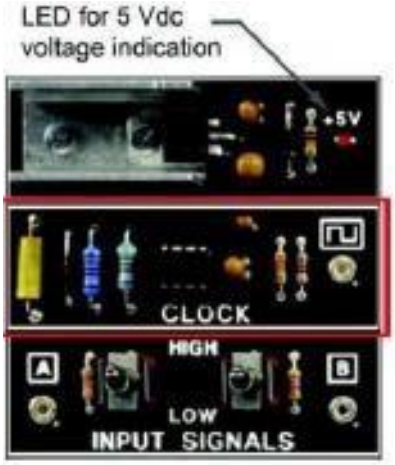
Examine the following circuit blocks: Three of the circuit blocks are located in the upper left corner of the circuit board.

The support circuit blocks include:

1- POWER SUPPLY



2- CLOCK



3- INPUT SIGNAL

- The ten circuit blocks that contain digital logic circuits are:
  1- AND/NAND circuit block
  2- OR/NOR circuit block
  3- XOR/XNOR circuit block
  4- OPEN COLLECTOR circuit block
  5- SET/RESET FLIP-FLOP circuit block
  6- D-TYPE FLIP-FLOP circuit block
  7- JK FLIP-FLOP circuit block
  8- TRI-STATE OUTPUT circuit block
  9- TTL/CMOS COMPARISON circuit block
  10- DATA BUS CONTROL circuit block.

- The ten digital logic circuit blocks are organized into the following lessons:
  - Fundamental Logic Elements
  - Exclusive OR and NOR Logic Functions
  - Open Collector and Other TTL Gates
  - SR- and D-type Flip-Flops
  - JK Flip-Flops
  - Tri-State Output
  - TTL and CMOS Comparison
  - Data Bus Control
  - Troubleshooting.

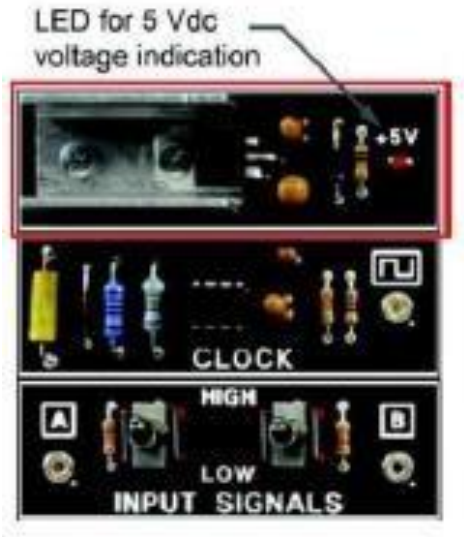
- _ _The INPUT SIGNALS and CLOCK circuit blocks

  a. demonstrate the functions of OR and NOR gates.
  b. provide static high and low signals and a dynamic square wave signal to the circuit blocks.

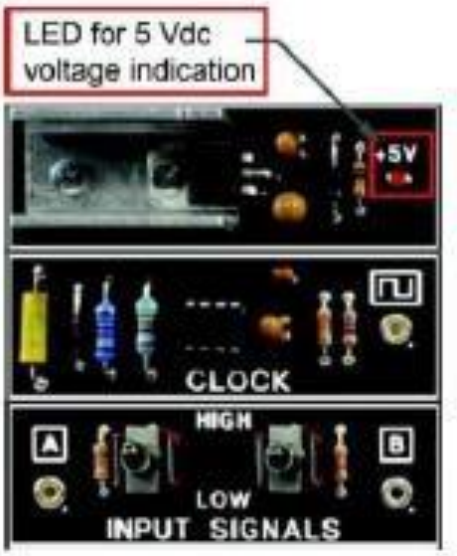
- **Power Supply Regulation**

The POWER SUPPLY REGULATOR circuit block, which is not labeled, is located above the CLOCK circuit block.

The power supply regulator converts the 15 Vdc supply to the base unit to a regulated 5 Vdc supply for the circuit board.

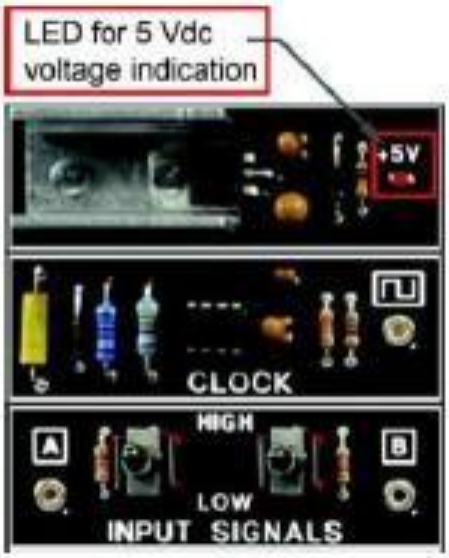


When the red LED on the right side of the circuit block is on (glowing), there is a 5 Vdc supply to the circuit blocks.



Be sure that the power supply regulator LED is always on when you do the exercise procedures. All the circuit blocks use a 5 V dc supply.

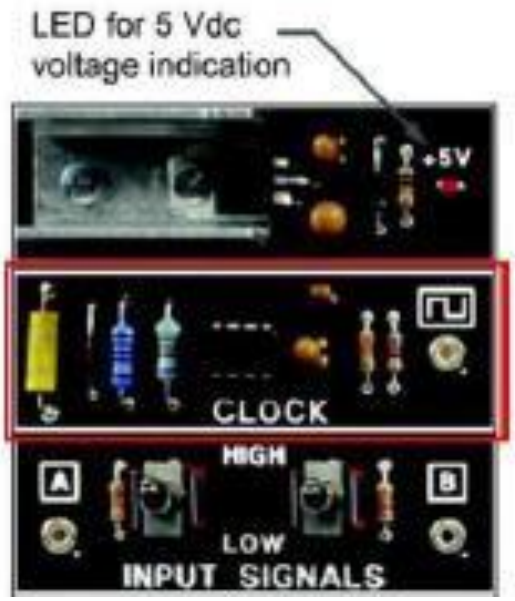
Note: The TTL/CMOS COMPARISON circuit block uses a 15 Vdc supply directly from the base unit.



Q: When the red LED is on (glowing) in the POWER SUPPLY REGULATOR circuit block,
a. 10 Vdc power is supplied to the circuits.
b. 5 Vdc power is supplied to the circuits.

- **Clock**

The CLOCK circuit block provides a square wave, 50 kHz pulse train signal with a 5 V peak-peak amplitude.

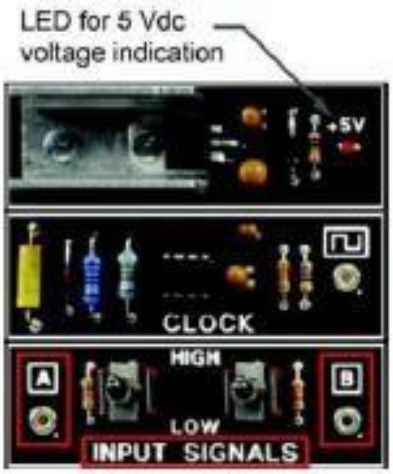


The output of the CLOCK is labeled with a square wave symbol.

The clock signal is used by several circuit blocks as a dynamic input signal.

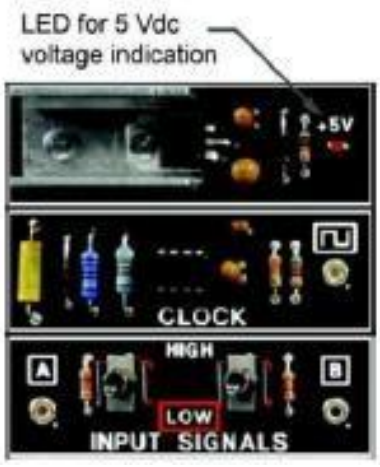
- **Input Signals**

The INPUT SIGNALS circuit block has two outputs labeled A and B.

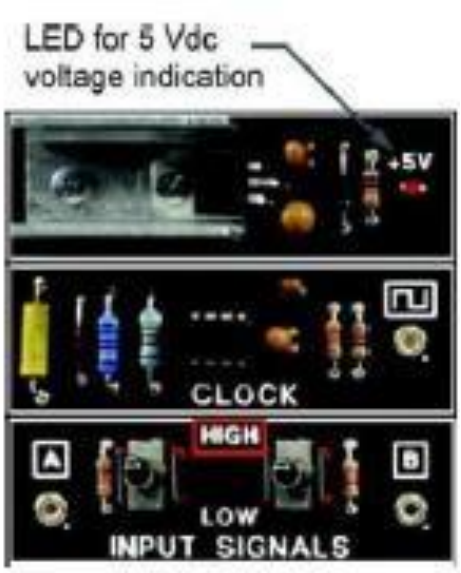


There is a toggle switch for each output.

When the toggle switch is in the LOW position, the output is at a logic 0, or low level (0 Vdc).



When the toggle switch is in the HIGH position, the output is at a logic 1, or high level (5 Vdc).



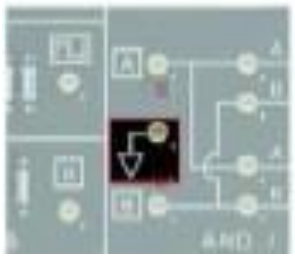
Outputs A and B of the INPUT SIGNALS circuit block are connected to inputs A and B of the circuit blocks during the procedural steps to provide either a logic 0 (0 Vdc) or a logic 1 (5 Vdc) input signal.

Test leads (interconnecting leads) are used to make the connections.

Q: When toggle switches A and B are in the HIGH position, the signal at the A and B terminals is
a. logic 1 (5 Vdc).
b. logic 0 (0 Vdc).

- **Ground Terminals**

Ground terminals on the circuit board are labeled with a ground symbol.



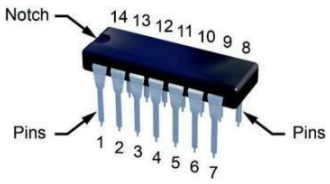
Ground terminals (0 Vdc) are located in several areas of the circuit blocks.

When using the multimeter or oscilloscope, be sure to connect the black common lead to a ground terminal on the circuit board.

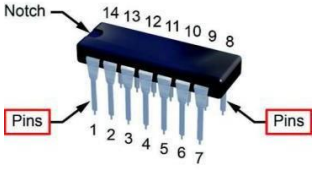
Q: The common lead of a multimeter or an oscilloscope should always be connected to
a. the B terminal of the INPUT SIGNALS circuit block.
b. one of the ground terminals on the circuit block.

- **Integrated Circuit Packages**

The digital logic circuits on the circuit board are contained in dual-in-line package (DIP) integrated circuit (IC) packages.

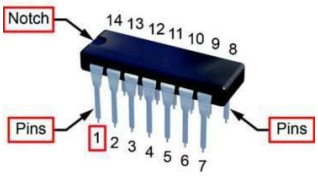


Dual-in-line package (DIP) means that the pins are positioned in a line on both sides of the IC package.



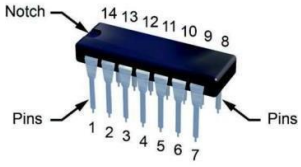
From the top side of the IC, pin 1 is located to the left of the notch, as shown below. The pins are numbered counterclockwise.

These IC packages usually contain several logic circuits of the same type.



Q: For an integrated circuit (IC), DIP means

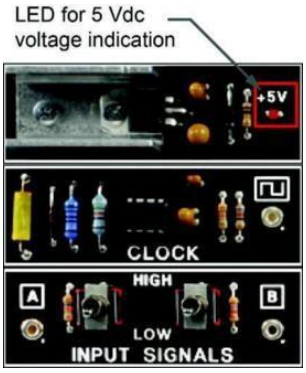
a. digital integrated pulse.
b. dual-in-line package.



PROCEDURE

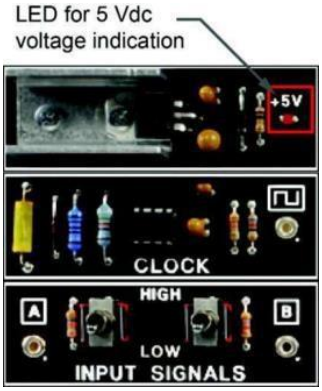
Q: In the POWER SUPPLY REGULATOR circuit block (upper left corner of the circuit board), is the LED on (glowing)?

a. yes
b. no

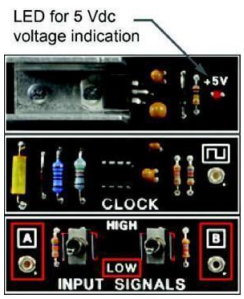


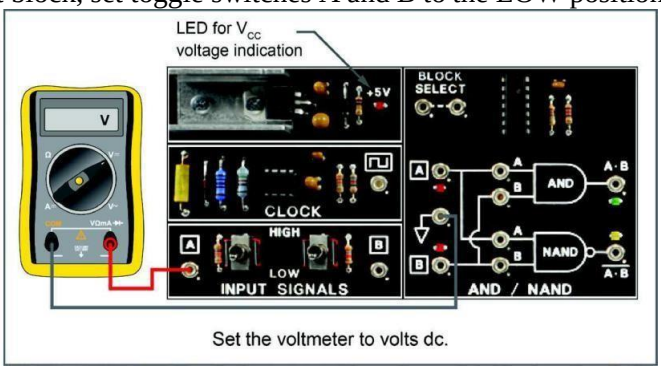
Q: When the POWER SUPPLY REGULATOR circuit block LED is on, the 15 Vdc supply to the base unit is

a. not being regulated to 5 Vdc.
b. being regulated to a 5 Vdc supply for the circuit board.
c. being supplied to the circuit board.



In the INPUT SIGNALS circuit block, set toggle switches A and B to the LOW position.

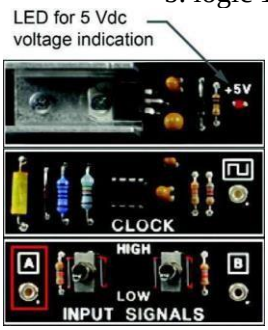




Connect the red (positive) lead of a voltmeter to the A terminal, and connect the black (negative) common lead to a ground terminal on the circuit board.

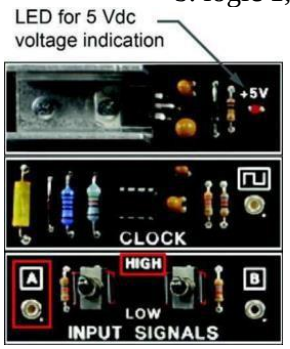
Q: The logic state of the A terminal is:

a. logic 0, or low (0 Vdc). b. logic 1, or high (5 Vdc).



Q: Change the position of toggle switch A to HIGH. The logic state of the A terminal is:

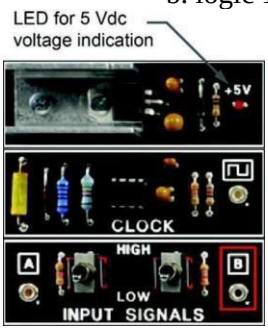
a. logic 0, or low (0 Vdc). b. logic 1, or high (5 Vdc).



Connect the red (positive) lead of a voltmeter to the B terminal. Leave the black (negative) common lead connected to the ground.

Q: The logic state of the B terminal is

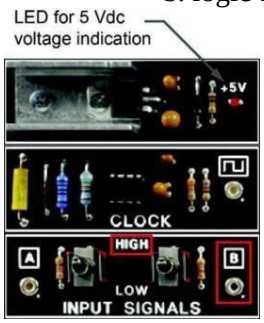
a. logic 0, or low (0 Vdc). b. logic 1, or high (5 Vdc).



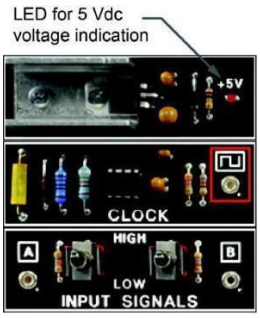
Change the position of toggle switch B to HIGH.

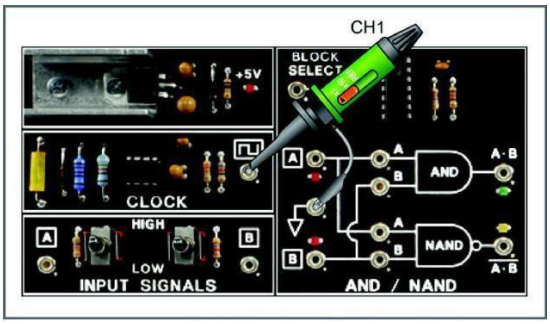
Q: The logic state of the B terminal is

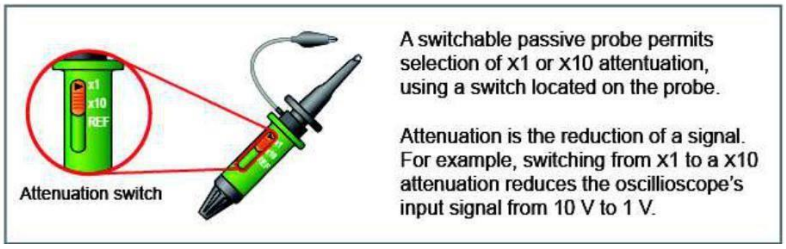
a. logic 0, or low (0 Vdc). b. logic 1, or high (5 Vdc).



Connect the channel 1 probe of the oscilloscope to the output terminal at the CLOCK circuit block. Connect the channel 1 probe ground clip to a ground terminal on the circuit board.

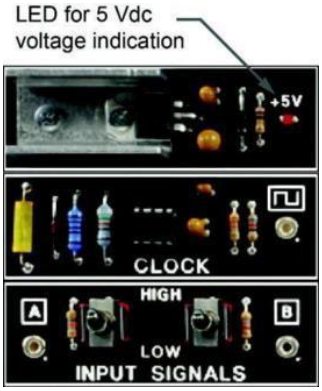






Set the channel 1 probe to X10, and set the channel 1 vertical sensitivity to 0.5 V/div. With these settings, each vertical division (Y-axis) on the oscilloscope screen is 5 V/div.

Set the sweep to 5 s/div and trigger on channel 1. With this setting, each horizontal division is 5 s/div.

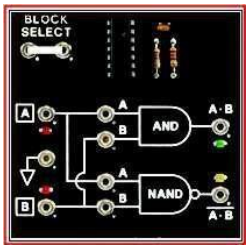


Q: The signal on channel 1 of the oscilloscope is a

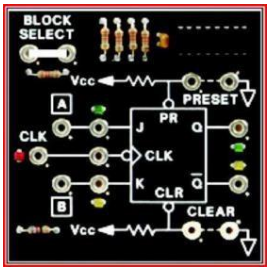
a. sine wave with a 5 Vpk-pk amplitude and a frequency of 50 kHz.

b. square wave with a 5 Vpk-pk amplitude and a frequency of 50 kHz.

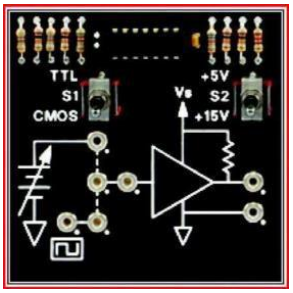
Q: The circuit shown here is the
a. AND/NAND circuit block. b. OR/NOR circuit block. c. XOR/XNOR circuit block.



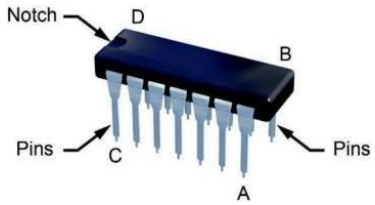
Q: This circuit shown is the
a. OPEN COLLECTOR circuit block. b. D-TYPE FLIP-FLOP circuit block.
c. JK FLIP-FLOP circuit block. d. SET/RESET FLIP-FLOP circuit block.



Q: This circuit shown here is the
a. TRI-STATE OUTPUT circuit block.
b. TTL/CMOS COMPARISON circuit block.
c. DATA BUS CONTROL circuit block.



Q: Pin 1 of the IC shown here is located at
a. A. b. B. c. C. d. D.



_ _CONCLUSION

• The DIGITAL LOGIC FUNDAMENTALS circuit board contains 13 circuit blocks.
• The POWER SUPPLY REGULATOR, CLOCK, and INPUT SIGNALS circuit blocks are support circuits to the ten circuit blocks that contain digital logic circuits.
• The +5 V LED indicates that 5 Vdc power is available to the circuit board.

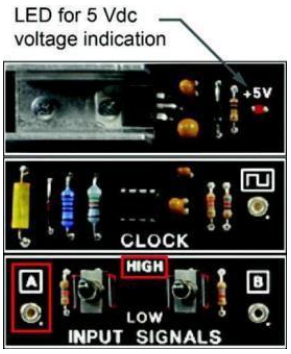
- The CLOCK circuit block provides a 50 kHz square wave clock signal.
- The INPUT SIGNALS circuit block provides two outputs (A and B) for providing static high (logic 1) and low (logic 0) signals to the other circuit blocks.
- The circuit board contains several ground terminals.
- The logic circuits on the circuit board are contained in dual-in-line (DIP) integrated circuit (IC) packages.

➢ REVIEW QUESTIONS

1. How can we ensure that the circuits in the DIGITAL LOGIC circuit board will work properly?
   a. Check that the 15 Vdc power supply is turned on.
   b. Check that toggle switches A and B are in the LOW position.
   c. Check that the +5 V LED is on (glowing).
   d. Check that the CM and fault switches are off.

2. Static logic 1 (high) and logic 0 (low) signals are obtained from the
   a. CLOCK circuit block.
   b. DATA BUS CONTROL circuit block.
   c. 15 Vdc power supply.
   d. INPUT SIGNALS circuit block.

3. If toggle switch A on the INPUT SIGNALS circuit block is set to the HIGH position, the signal at the A output is:
   a. logic 0. b. in a high-Z state. c. logic 1. d. a 50 kHz square wave.



4. When using an oscilloscope to observe a signal, connect the oscilloscope probe ground (common) clip to
   a. the output terminal on the CLOCK circuit block.
   b. one of the ground terminals on the circuit board.
   c. the B output terminal on the INPUT SIGNALS circuit block.
   d. a terminal with a 5 Vdc output.

5. The DIGITAL LOGIC FUNDAMENTALS circuit board contains how many circuit blocks that have logic circuits?
   a. 10 b. 13 c. 12 d. 11

Lab 1B: Basic Digital Simulation

➢ Objectives:

- To learn the basic digital simulation and verify selected circuits using digital circuit simulator called "Deeds" (Digital Electronics Education and Design Suite) simulator.
- In this introductory exercise you will test the simple logic network represented in the figure below and, at the same time, you will gain confidence with the Digital Circuit Simulator (d-DcS) of the Deeds.
- Note: you can try the different inputs and output devices in the simulator.

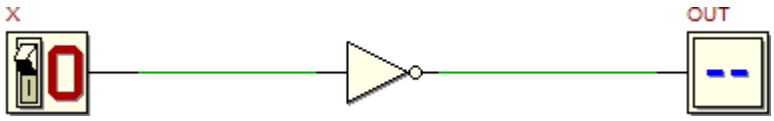
➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

➢ Background:

Deeds: Digital Electronics Education and Design Suite is a set of educational tools for Digital Electronics. It covers various areas of digital electronics including combinational logic networks, sequential logic networks, custom circuit blocks design, micro-computer programming. The program helps students learn to design and test electronic systems and digital systems on FPGA boards.

1: Use the simulator to draw the following circuit.



2: check the behavior of the network

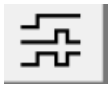
Start the functional simulation (Interactive Animation) of the network by clicking, on the DcS toolbar, the command 

Now the input switch can be toggled and the gate's output OUT will change accordingly.

3: Fill the output (OUT) column with the data resulting from the simulation.

X	OUT
0	
1	

4: timing simulation of the same network

Start the timing simulation of the network by clicking, on the d-DcS toolbar, the command 

The input values must be drawn directly on the timing diagram window. You should define the

values versus time of the input as shown in the figure above. Then draw the resulted output on the following figure.

Lab 2A: AND-NAND Logic Functions

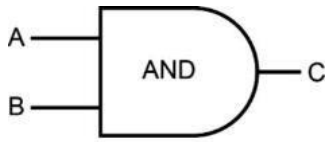
- **OBJECTIVE**

  When you have completed this exercise, you will be able to determine the operation of the AND and NAND logic gates. You will verify the results by generating truth tables for each function.

- **Requirements**
  - DIGITAL LOGIC FUNDAMENTALS (LabVolt) Circuit Board
  - PC or Laptop
  - A multimeter
  - An oscilloscope

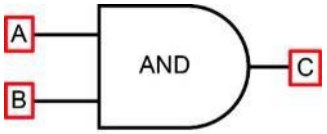
- **EXERCISE DISCUSSION**

The schematic symbol of a two-input AND gate and the Boolean equation for the AND gate are shown here.



C = A•B

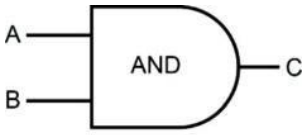
Input signals are labeled A and B, and the output is labeled C.



C = A•B

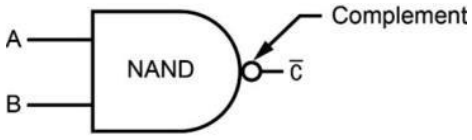
The Boolean equation for the AND gate states that C is high when A and B are both high. The AND operation is indicated by the dot between A and B.

NOTE: A•B and AB without the "•" are identical.



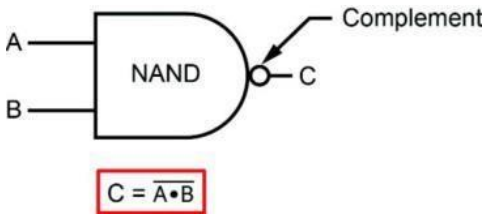
C = A•B

The schematic symbol of a two-input NAND gate and the Boolean equation for the NAND gate are shown here.

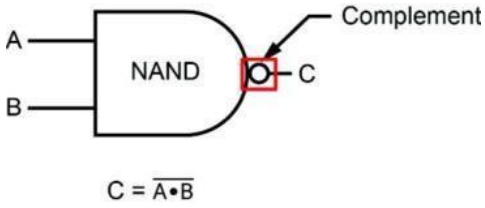


$\overline{C} = A \cdot B$

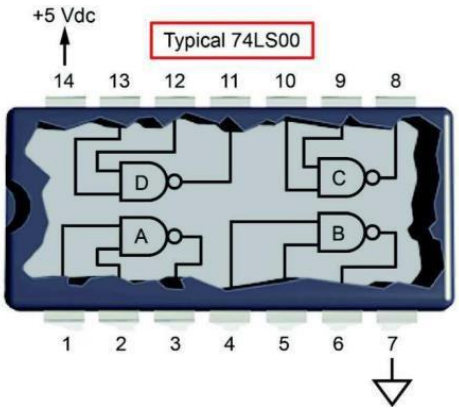
The Boolean equation for the NAND gate states that C is low when A and B are both high. The bar over A·B represents the complement.



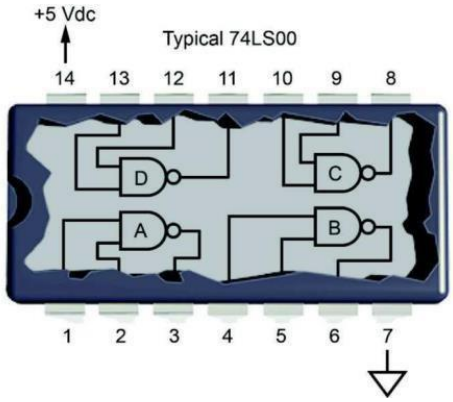
The NAND gate function has a bubble drawn at the output side of the gate. The bubble indicates a complement.



The following diagram relates to the pin layout of an IC chip on the circuit board.

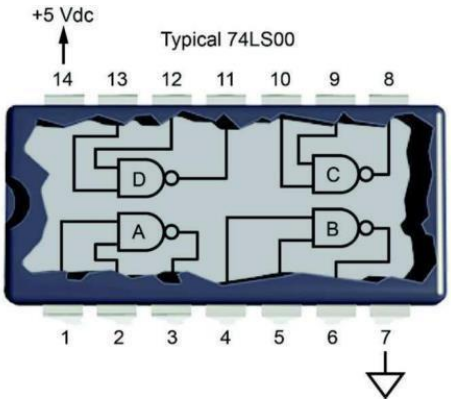


Pins 14 and 7 supply power to the IC. The IC provides four separate two-input NAND gates labeled A through D.



Q: Pin 11 is the output for which gate?

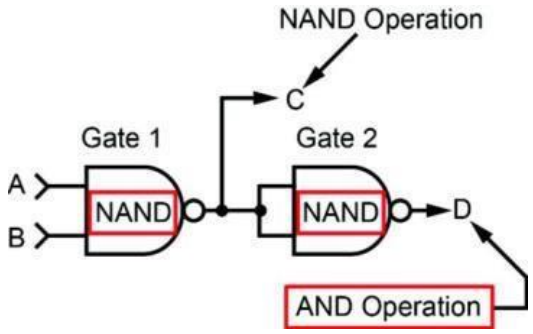
a. A b. B c. C d. D



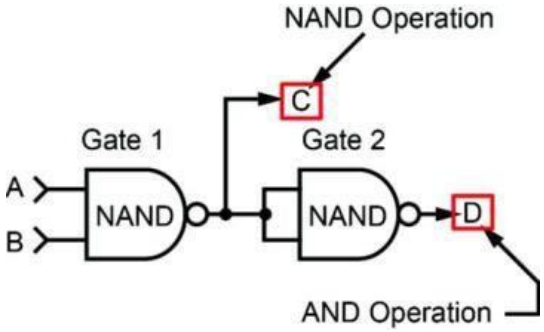
For the 74LS00 IC, inputs may be tied to other inputs, or outputs may be connected to inputs; however, outputs cannot be connected to one another.

Unused inputs generally are pulled high (connected to 5 Vdc) through a pull-up resistor.

Two NAND gates can be cascaded (connected in series) to generate an AND operation, as shown.



Output C provides a NAND response to circuit inputs A and B. Output C is complemented by the action of GATE 2. In turn, this gate generates an AND operation for circuit inputs A and B at output D.



This is the truth table for the circuit shown above.

Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

Complements

Outputs C and D are complements. Output column C provides the NAND function truth table, while output column D provides the AND function truth table.

Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

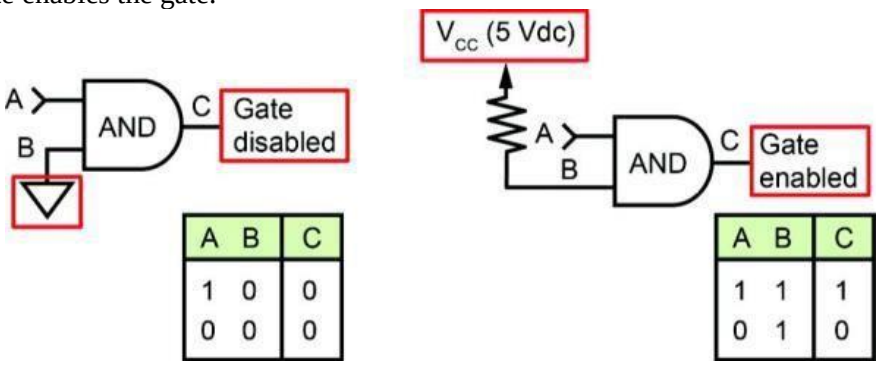
Complements

A and B are the two inputs to the circuit. Four unique input conditions test all possible input combinations.

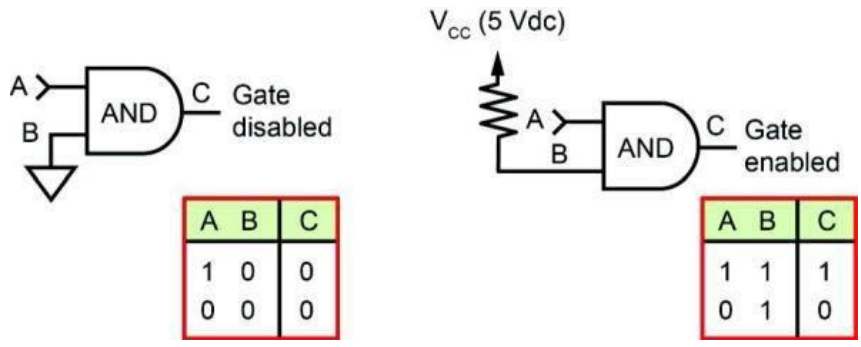
Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

Complements

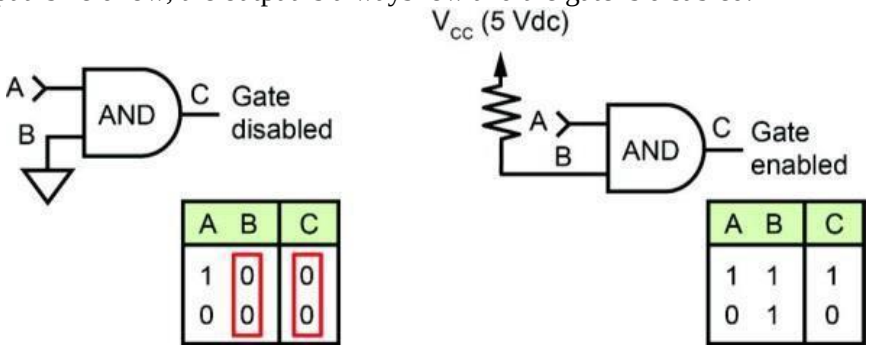
A low logic state at any input disables an AND gate. A high logic state at any input of a two-input AND gate enables the gate.



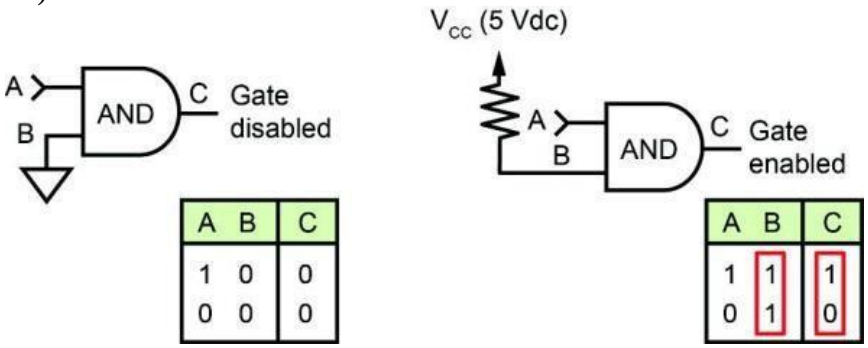
The disable and enable combinations and the truth tables for an AND gate are shown here.
Note: Gate "enabled" means that the gate output follows one of its inputs.



If one input is held low, the output is always low and the gate is disabled.

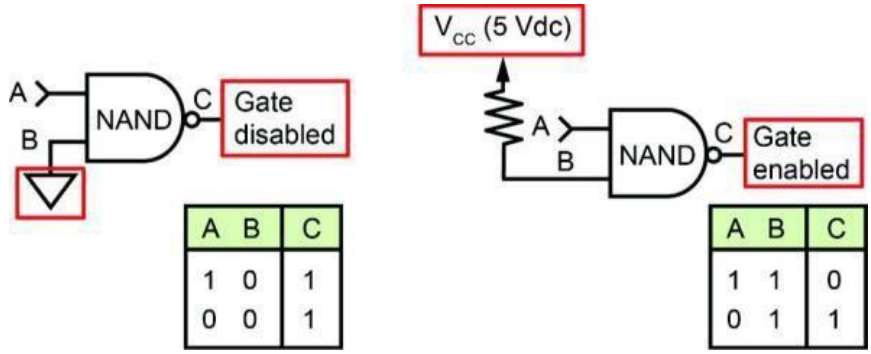


If one input is held high, the output is the same level as the other input and the gate is enabled (e.g. C follows A).

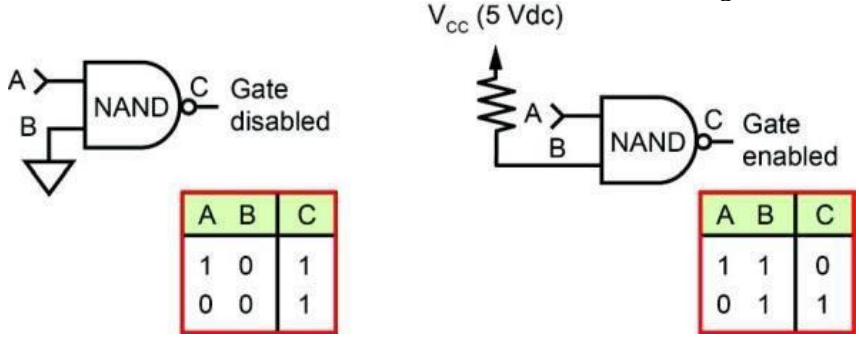


Q: If you wanted to disable an AND gate, you would pull one input
a. high. b. low.

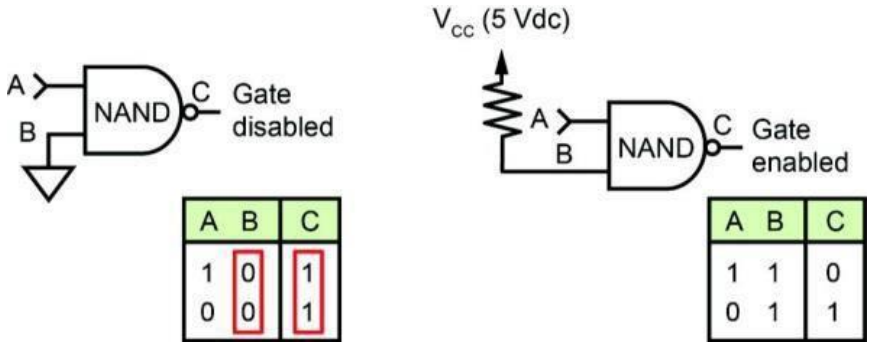
A low level at any input disables a NAND gate. A high level at one input of a NAND gate enables the gate.



The disable and enable combinations and the truth tables for a NAND gate are shown here.



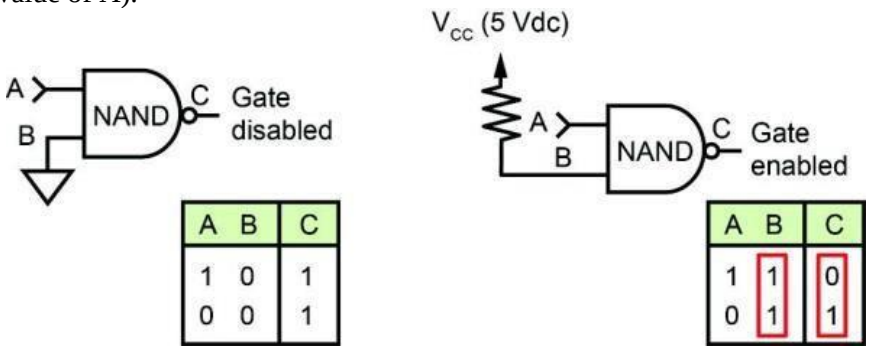
A disabled NAND gate locks out its other input and generates a high level (1) output, as shown in the truth table.



A	B	C
1	0	1
0	0	1

A	B	C
1	1	0
0	1	1

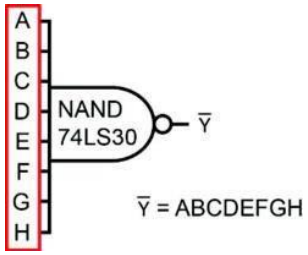
An enabled NAND gate complements the other input, as shown in the truth table (e.g. C takes the opposite value of A).



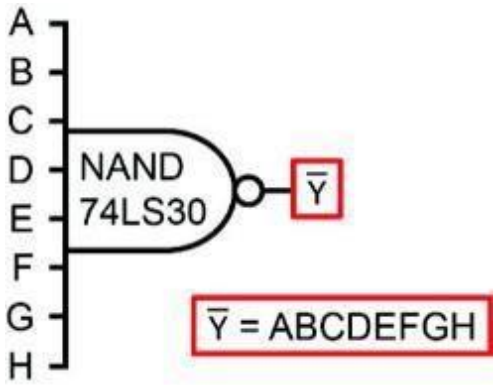
A	B	C
1	0	1
0	0	1

A	B	C
1	1	0
0	1	1

An eight-input NAND gate (74LS30) is shown. The operating principles of a two-input NAND gate apply to gates having more than two inputs.



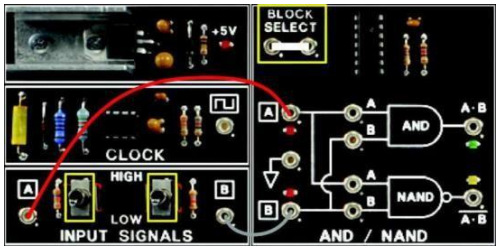
The output of this gate is low only when all inputs are high. Any one input at a low level locks out the other inputs (the output is always high).



PROCEDURE

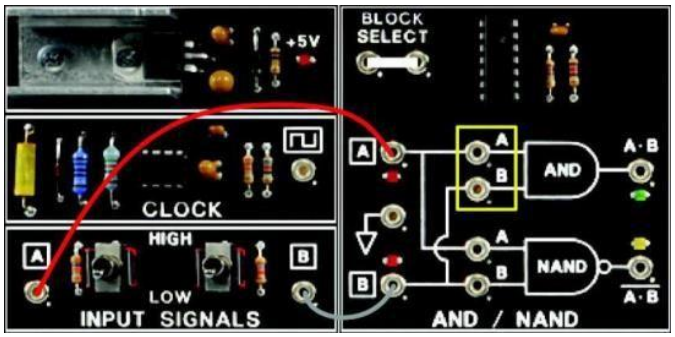
Locate the AND/NAND circuit block, and connect the circuit shown. Activate BLOCK SELECT. Place both toggle switches in the LOW position.

NOTE: A high logic level turns on an LED. You can verify the state of a signal, as indicated by a circuit LED, by connecting your multimeter to the appropriate test point.



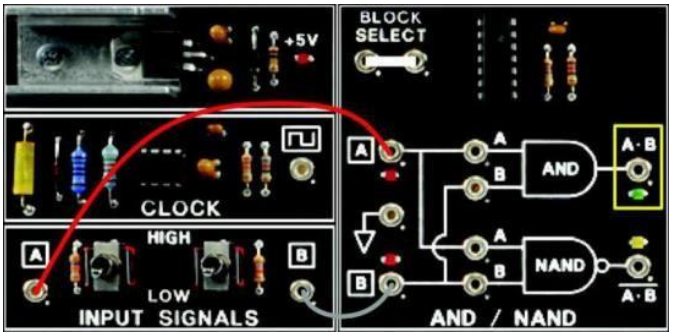
Q: What are the logic levels at AND gate inputs A and B?

a. both low b. both high



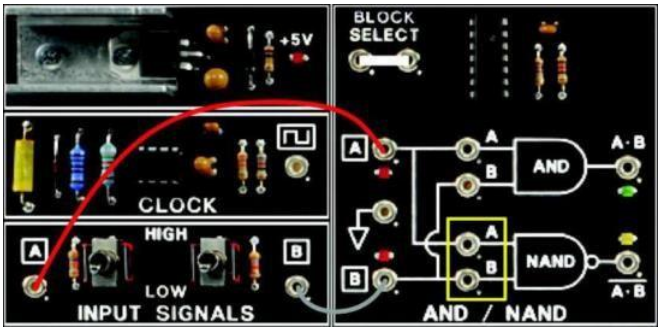
Q: Based on the input levels, what is the AND gate output level?

a. 1 b. 0



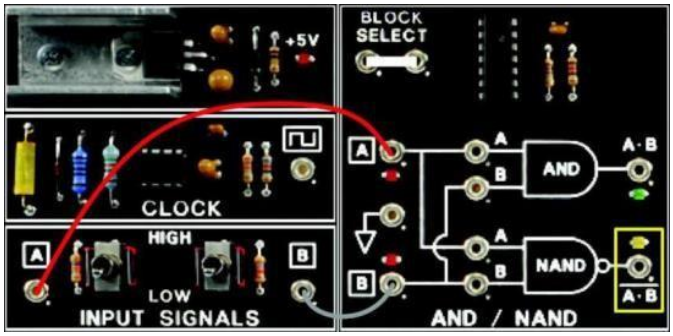
Q: What are the logic levels at the NAND gate inputs?

a. both low b. both high



Q: What is the logic level at the output of the NAND gate?

a. 1 b. 0



The table shows the AND and NAND outputs when inputs A and B are low.

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0	0	0	1

Place toggle switch A in the HIGH position.

Q: What is the AND gate output?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0	0	0	1
1	0	?	

Q: What is the NAND gate output?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0	0	0	1
1	0	0	?

Place toggle switch A in the LOW position and switch B in the HIGH position.
Q: What is the AND gate output?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	?	

Q: What is the output of the NAND gate?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	?

Set both switches A and B high.
Q: What is the AND output?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	?	

Q: What is the NAND gate output?

a. 1 b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	?

Q: Based on the truth table, when is the AND gate output high?

a. when any input is high b. when both inputs are high

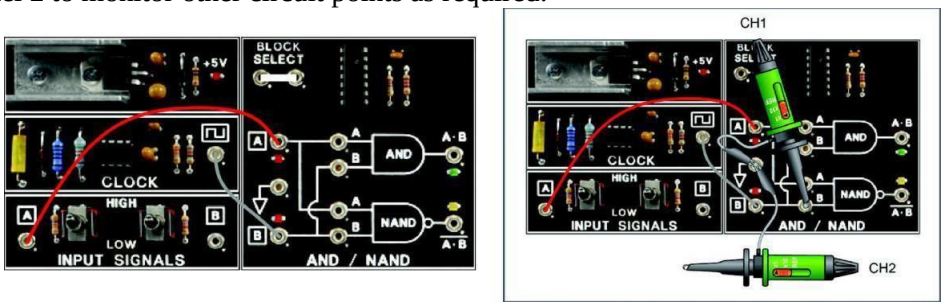
Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Q: Based on the truth table, are the outputs of the AND and NAND gates complementary?

a. yes b. no

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Connect the circuit shown here. Connect channel 1 of your oscilloscope to circuit input B. Use channel 2 to monitor other circuit points as required.



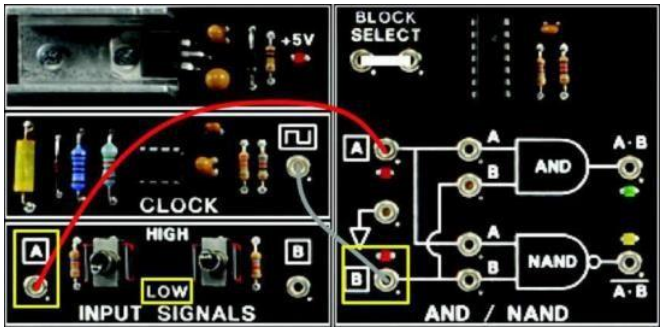
NOTE: LEDs will appear to be constantly on due to the pulse train input signal. This action does not alter the expected circuit operation. You may disable the circuit block LEDs by removing BLOCK SELECT.

Place switch A in the LOW position. Circuit input signal B is a square wave pulse train as seen on oscilloscope channel 1.

Monitor the AND gate and NAND gate outputs on channel 2 of the scope.

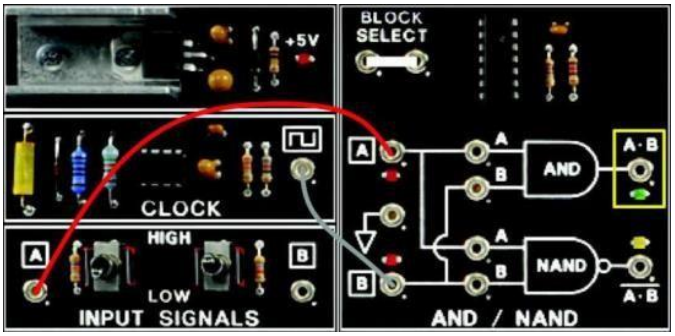
Q: Are the gates enabled or disabled?

a. enabled b. disabled



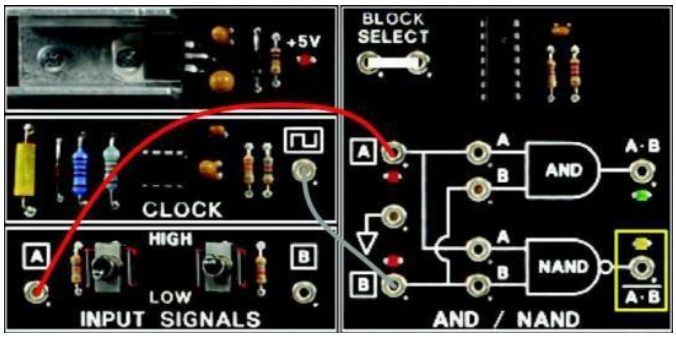
Q: Is the AND gate output high or low?

a. high b. low



Q: Is the NAND gate output high or low?

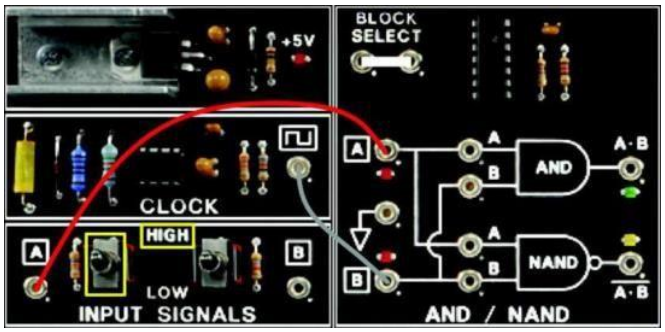
a. high b. low



Place switch A in the HIGH position. Monitor the output of each gate.

Q: Are the gates enabled or disabled by the high input at A?

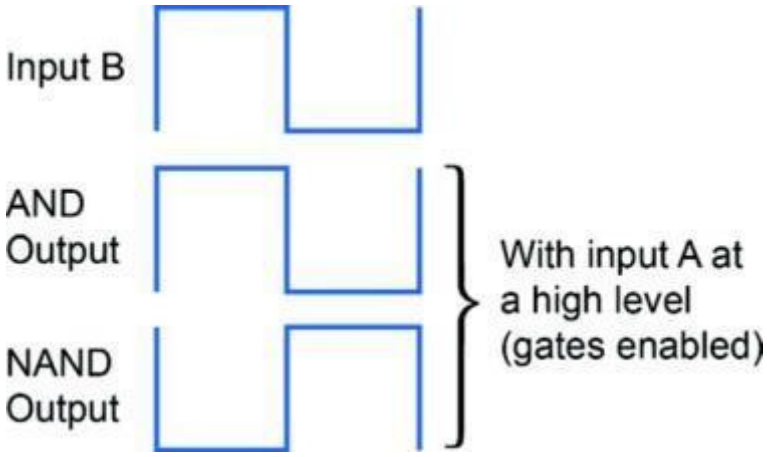
a. enabled b. disabled



Refer to the waves shown here, and compare the circuit outputs with the circuit input.

Q: With respect to input signal B, the AND output is

a. in phase. b. out of phase.



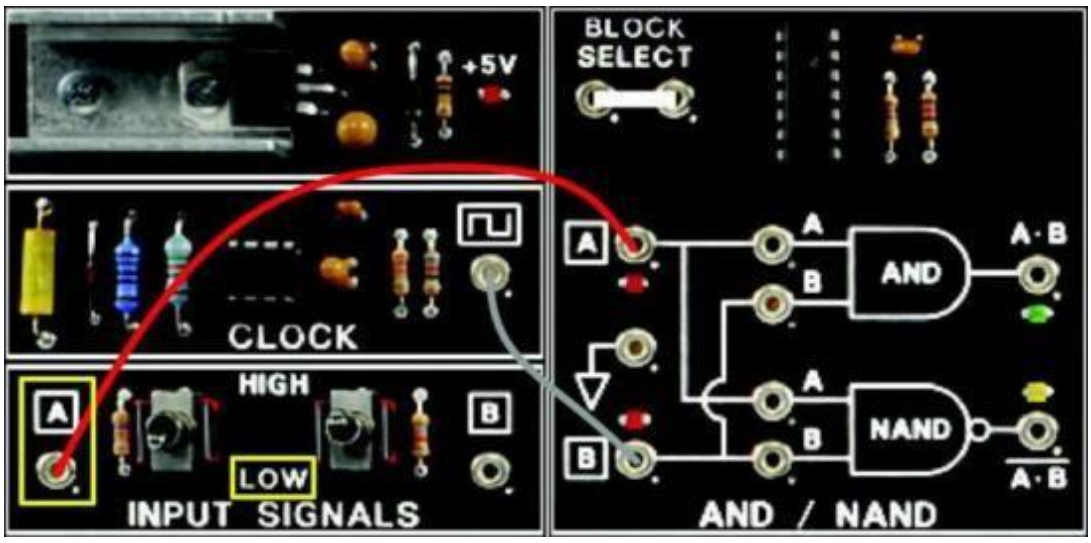
Q: With respect to input signal B, the NAND gate output is
a. in phase. b. out of phase.

➢ CONCLUSION

- The output of an AND gate is high only when all inputs are high.
- The output of a NAND gate is low only when all inputs are high.
- A low input disables an AND or a NAND gate.
- A high input (two-input gate) will enable an AND or a NAND gate.
- The output of an enabled AND gate is in phase with its input.
- The output of an enabled NAND gate is the complement of its input.

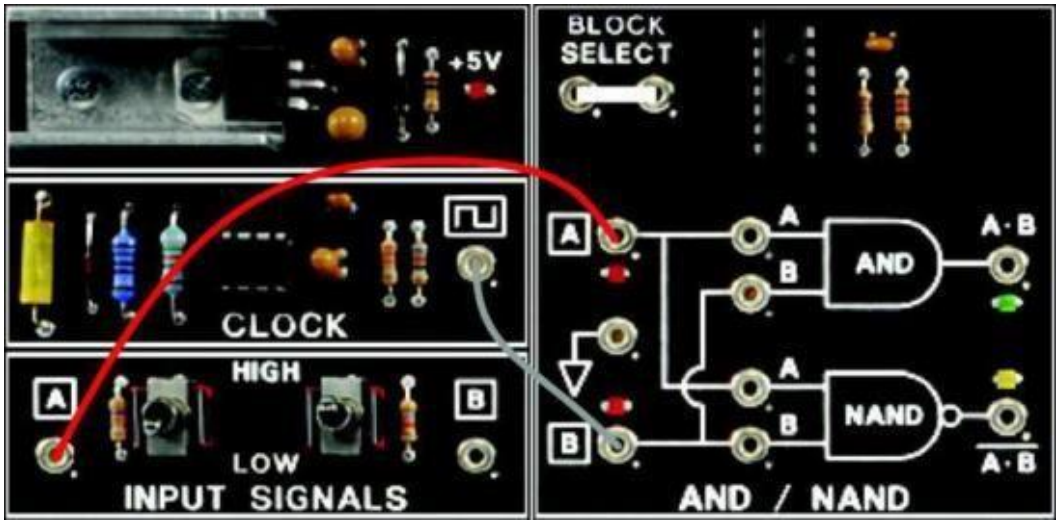
➢ REVIEW QUESTIONS

1. Locate the AND/NAND circuit block and connect the circuit shown. Disable the circuit gates by placing toggle switch A in the LOW position.



Place CM switch 6 in the ON position. The CM:
a. enables the NAND gate but not the AND gate.
b. disables the clock signal at input B.
c. enables the AND and NAND gates.
d. causes the AND and NAND gate outputs to be in phase.

2. Place CM switch 7 in the ON position. The CM:
    a. places a logic 1 signal at input B to the gates.
    b. prevents the gates from responding to changes at input A.
    c. enables the AND gate but disables the NAND gate.
    d. enables the NAND gate but disables the AND gate.



3. The output of an AND gate is high
    a. all of the time.
    b. when any input is low.
    c. when any input is high.
    d. when all inputs are high.

Lab 2B: OR-NOR Logic Functions

➢ OBJECTIVE

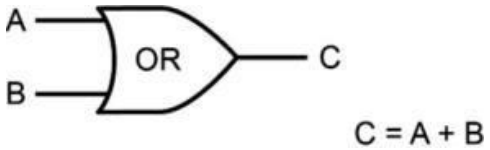
When you have completed this exercise, you will be able to determine the operation of the OR and NOR logic gates. You will verify your results by generating truth tables for each function.

➢ REQUIREMENTS

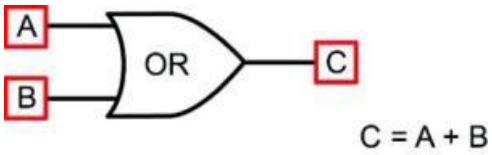
- DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
- PC or Laptop computer.
- A multimeter
- An oscilloscope

➢ EXERCISE DISCUSSION

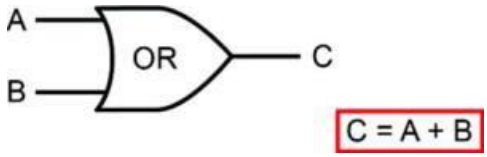
The schematic symbol of a two-input OR gate and the Boolean equation for the OR gate are shown.



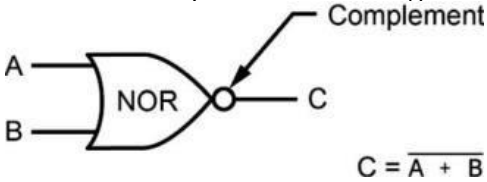
Input signals are labeled A and B, and the gate output is labeled C.



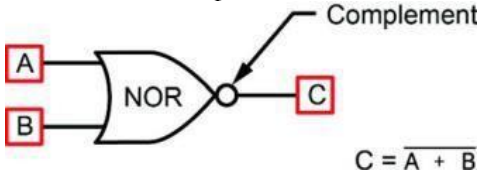
The Boolean equation for the OR gate states that C is high when A or B is high. In the equation, the + symbol indicates the OR function.



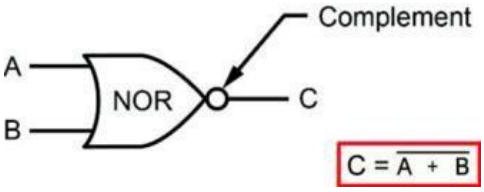
The schematic symbol and the Boolean equation for a NOR gate are shown here.



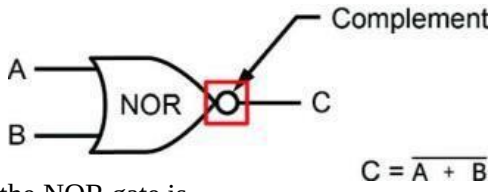
The inputs are labeled A and B, and the output is labeled C.



The Boolean equation for the NOR gate states that C is low when A or B is high. The bar over the A+B indicates the complement.



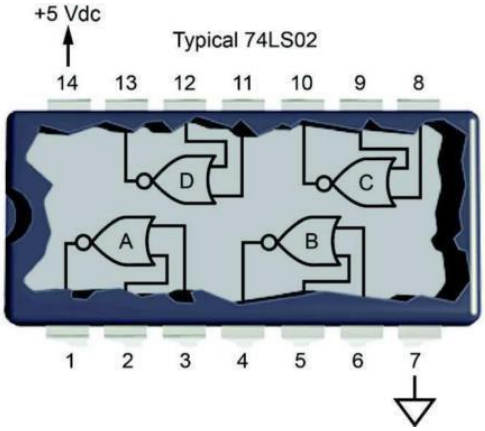
The NOR gate symbol has a bubble at the output of the gate. This bubble indicates a complement.



Q: The Boolean equation for the NOR gate is

a. C = A + B. b. C = A+B.

The following diagram shows an IC that contains four NOR gates.

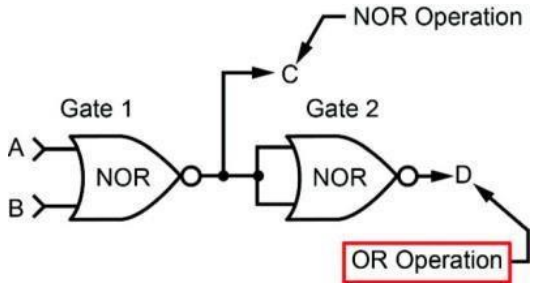


Pins 14 and 7 supply power to the IC. The IC provides four separate two-input NOR gates labelled A through D. For the 74LS02 IC, inputs may be tied to other inputs, and an output may be connected to inputs; however, outputs cannot be connected to one another.

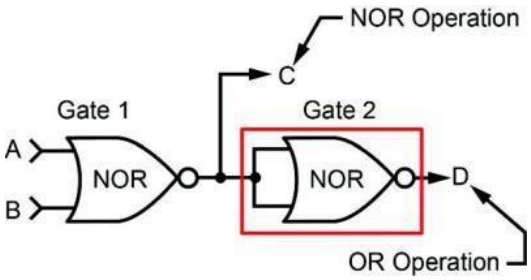
Pin 1 is the output to which gate?

a. A b. B c. C d. D

Two NOR gates can be cascaded (connected in series) to generate an OR operation, as shown.



Output D represents the OR function because of the complementary action of GATE 2.

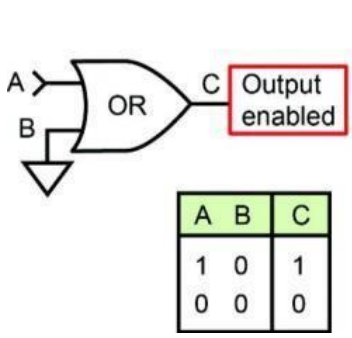


This is the truth table for the circuit. The outputs are complementary. Output column C provides the NOR function truth table, and output column D provides the OR function truth table for inputs A and B.

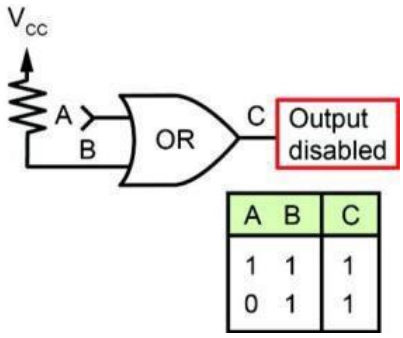
Inputs		Outputs	
		NOR	OR
A	B	C	D
1	1	0	1
1	0	0	1
0	1	0	1
0	0	1	0

Complements

The disable and enable combinations and the truth tables for an OR gate are shown here.

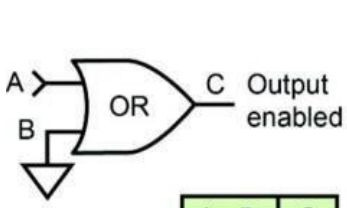


A	B	C
1	0	1
0	0	0

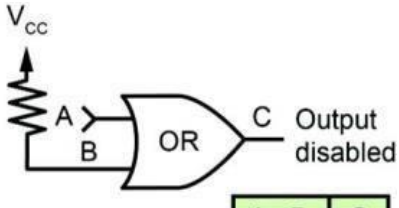


A	B	C
1	1	1
0	1	1

When one input is low, the OR gate is enabled and the output depends on the other input level.
Note: Gate "enabled" means that the gate output follows one of its inputs.

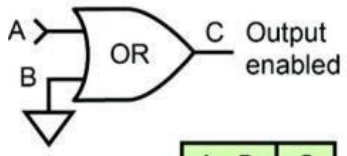


A	B	C
1	0	1
0	0	0

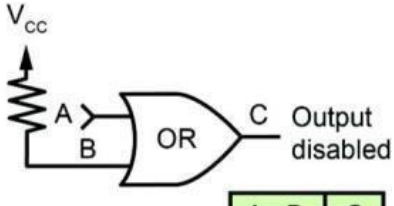


A	B	C
1	1	1
0	1	1

When one input is high, the output is disabled because it is always high independent of the level at the other input.

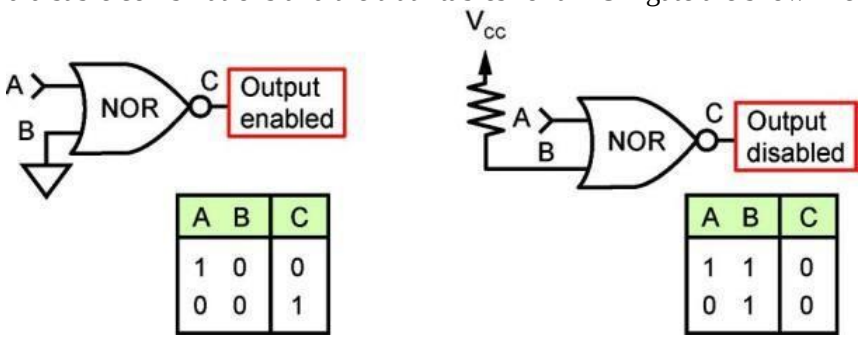


A	B	C
1	0	1
0	0	0

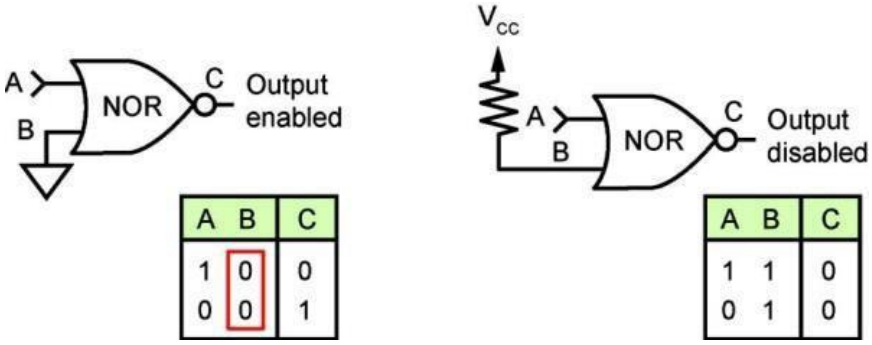


A	B	C
1	1	1
0	1	1

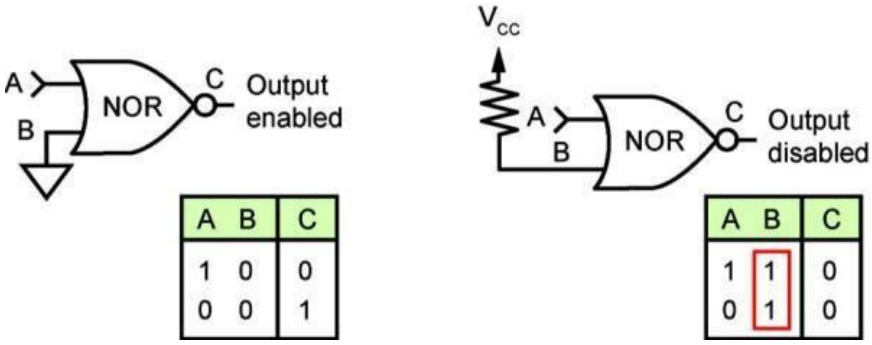
The enable and disable combinations and the truth tables for a NOR gate are shown here.



When one input is held low, the NOR gate is enabled and the output is the complement of the other input.



When one input is held high, the NOR gate is disabled. The output is always low independent of the other input level.



Q: If one input of an OR gate is held low, is the gate enabled or disabled?

a. enabled b. disabled

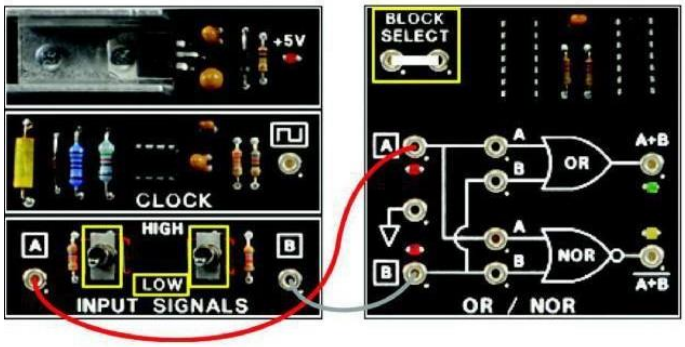
Here is a three-input NOR gate, the 74LS27. The operating principles of a two-input OR or NOR gate apply to gates having more than two inputs.

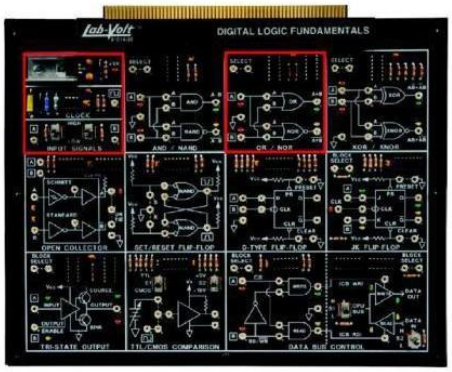
$$Y = \overline{A + B + C}$$

The output of this gate is low when any input is high. Any one input at a high level locks out the other inputs since the output is always low. When all inputs are low, the output is high.

PROCEDURE

Locate the OR/NOR circuit block, and connect the circuit shown. Activate BLOCK SELECT. Place both toggle switches in the LOW position.

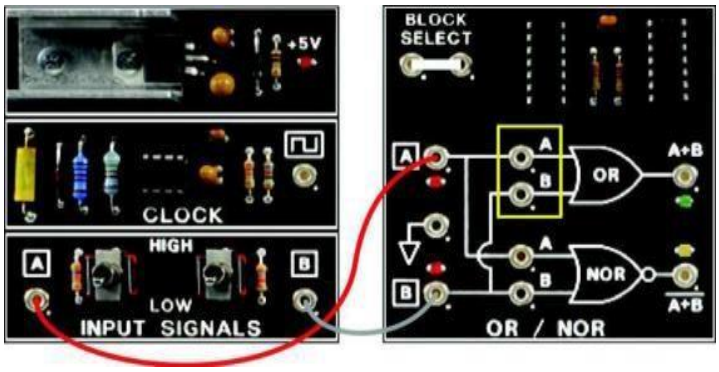




NOTE: A high logic level turns on an LED. You can verify the static state of a signal, as indicated by a circuit LED, or by connecting either your multimeter or oscilloscope to the appropriate point. To verify the state of a dynamic signal (square wave) an oscilloscope is used.

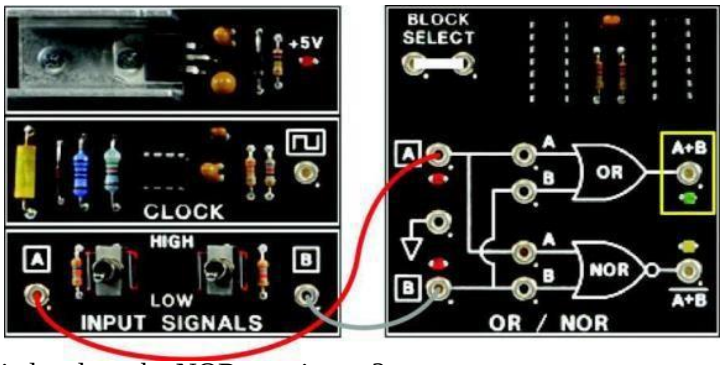
Q: What are the logic levels at the OR gate inputs?

a. both low b. both high



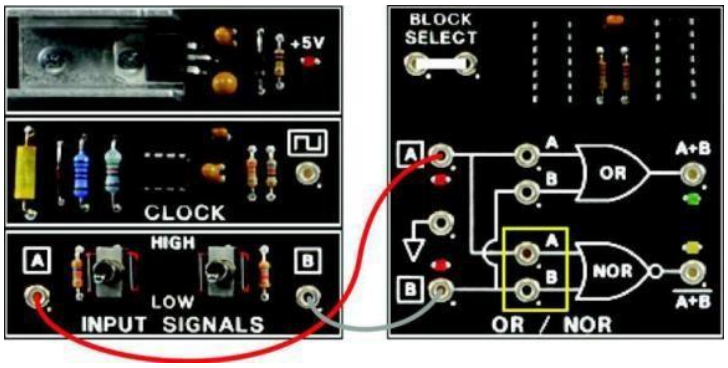
Q: What is the logic level at the output of the OR gate?

a. 1 b. 0



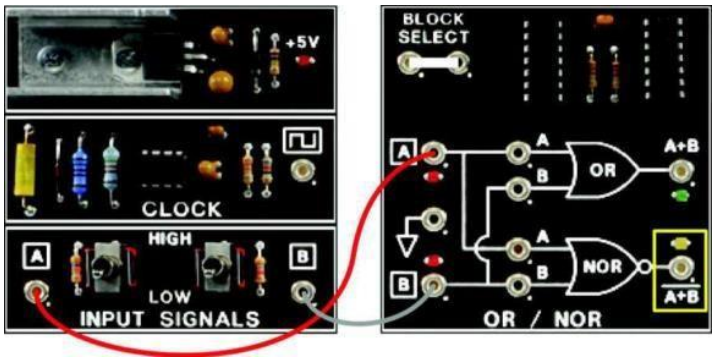
Q: What are the logic levels at the NOR gate inputs?

a. 1 b. 0



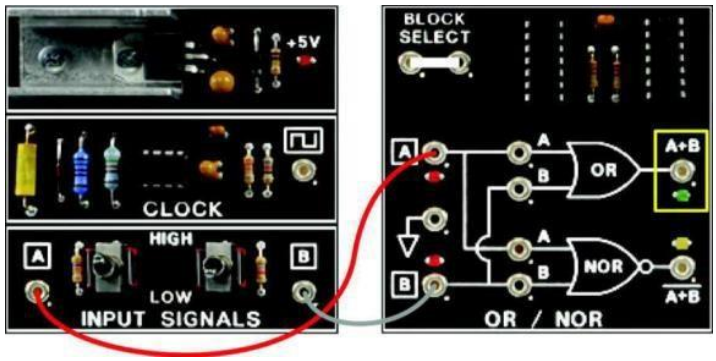
Q: What is the output level of the NOR gate?

a. 1 b. 0



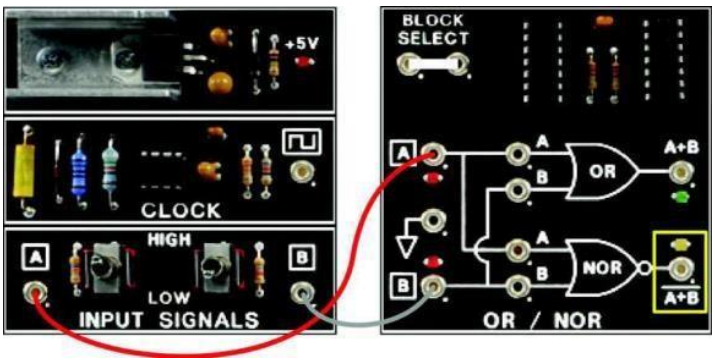
Q: If either toggle switch A or B (not both) were placed in the HIGH position, would the OR gate output be locked high or low?

a. high b. low



Q: If either toggle switch A or B (not both) were placed in the HIGH position, would the NOR gate output be locked high or low?

a. high b. low



The table shows the OR and NOR outputs when both A and B are low.

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \bullet B}$
0	0	0	1

Q: Place toggle switch A in the HIGH position and switch B in the LOW position. What is the OR gate output?

a. 1 b. 0

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \bullet B}$
0 1	0 0	0 ?	1

Q: Leave toggle switch A in the HIGH position and switch B in the low position. What is the NOR gate output?

a. 1 b. 0

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \bullet B}$
0 1	0 0	0 1	1 ?

Q: Place toggle switch A in the LOW position and switch B in the HIGH position. What is the OR gate output?

a. 1 b. 0

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \bullet B}$
0 1 0	0 0 1	0 1 ?	1 0

Q: Leave toggle switch A in the LOW position and switch B in the HIGH position. What is the NOR gate output?

a. 1 b. 0

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	1	0
0	1	1	?

Q: Place toggle switch A in the HIGH position and switch B in the HIGH position. What is the OR gate output?

a. 1 b. 0

Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	?	

Q: Place toggle switches A and B in the HIGH position. What is the NOR gate output?

a. 1 b. 0

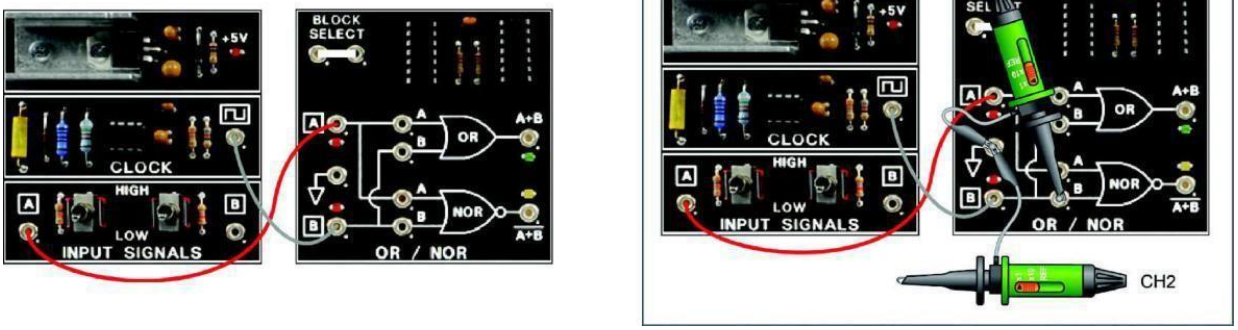
Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	?

Q: Based on the truth table, when is the NOR gate output high?

a. when both inputs are low b. when any input is low c. when any input is high

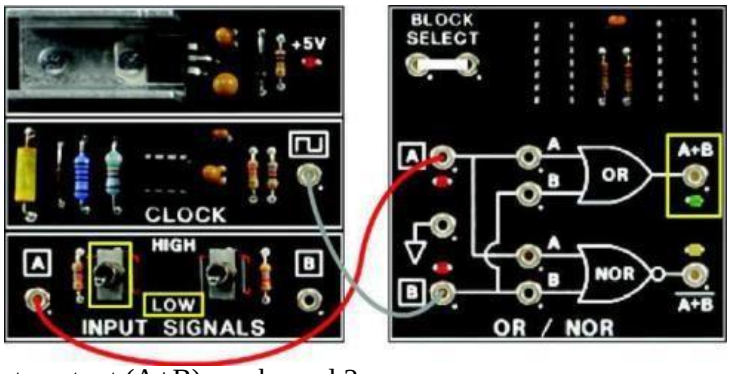
Inputs		Outputs	
		OR	NOR
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

Modify your test circuit as shown. Connect channel 1 of your oscilloscope to circuit input B. Use channel 2 to monitor other circuit points as required.



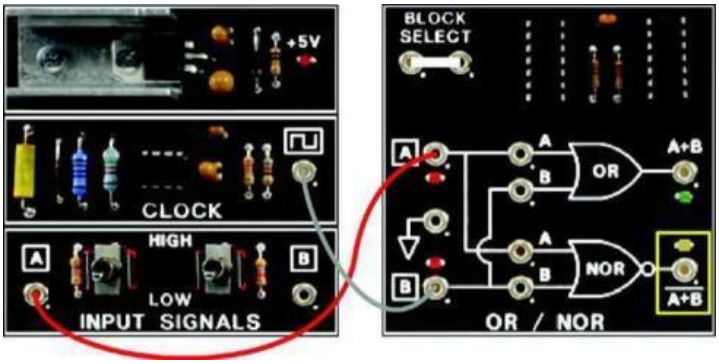
Place switch A in the LOW position. The circuit input signal is a square wave as seen on oscilloscope channel 1. Monitor the OR gate output (A + B) on channel 2.

Q: The OR gate output is: a. enabled. b. disabled.



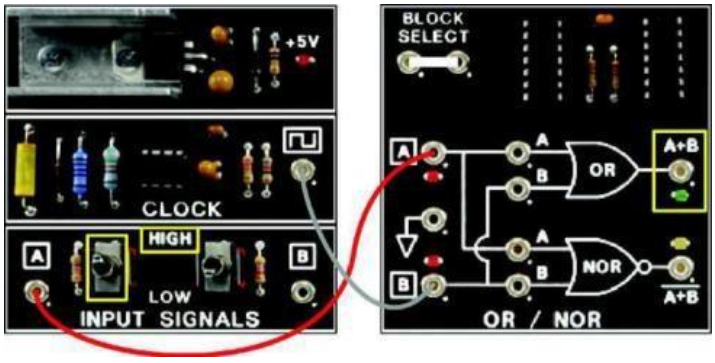
Monitor the NOR gate output (A+B) on channel 2.

Q: The NOR gate output is : a. enabled. b. disabled.

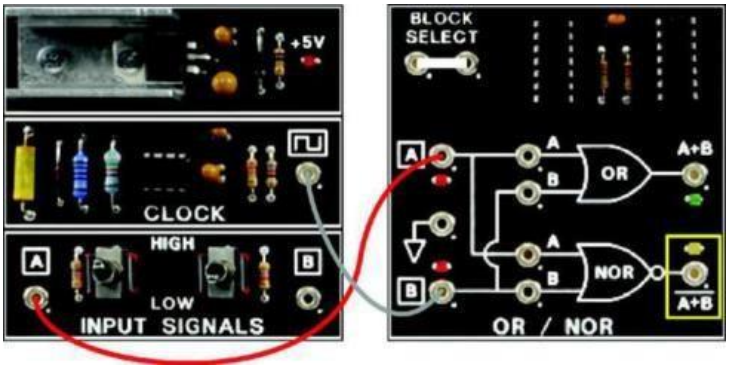


Place switch A in the HIGH position. Monitor the output of the OR gate.

Q: The gate is: a. enabled. b. disabled.



Monitor the output of the NOR gate.
Q: The gate is : a. enabled. b. disabled.

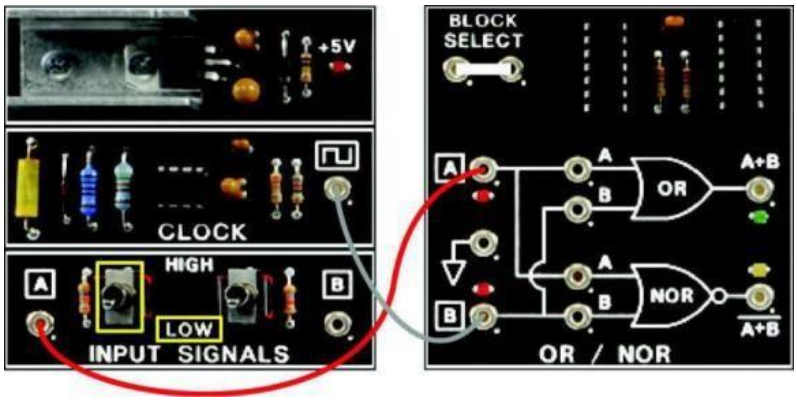


➢ CONCLUSION

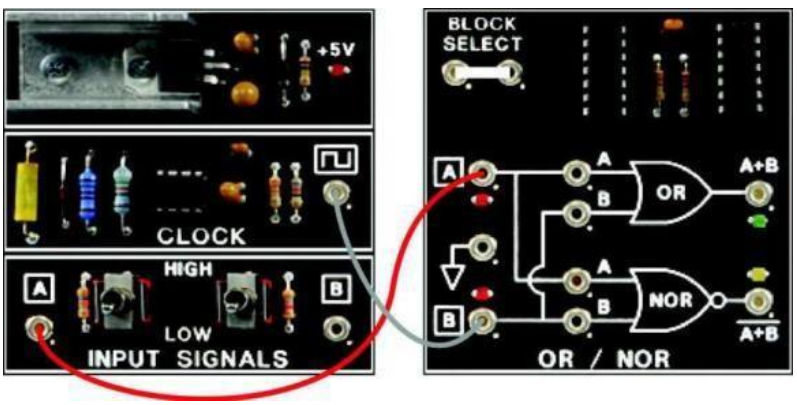
- The output of an OR gate is high when any input is high.
- The output of a NOR gate is low when any input is high.
- A high input will disable an OR or a NOR gate.
- A low input (two-input gate) will enable an OR or a NOR gate.
- OR/NOR gate outputs complement each other.

➢ REVIEW QUESTIONS

1. Locate the OR/NOR circuit block, and connect the circuit shown. Enable the circuit gates by placing toggle switch A in the LOW position.



Place CM switch 13 in the ON position. With the CM activated, the OR gate and NOR gate:
a. outputs follow input signal B. b. input B signals are locked out.
c. functions are affected by switch A. d. outputs are no longer complementary.

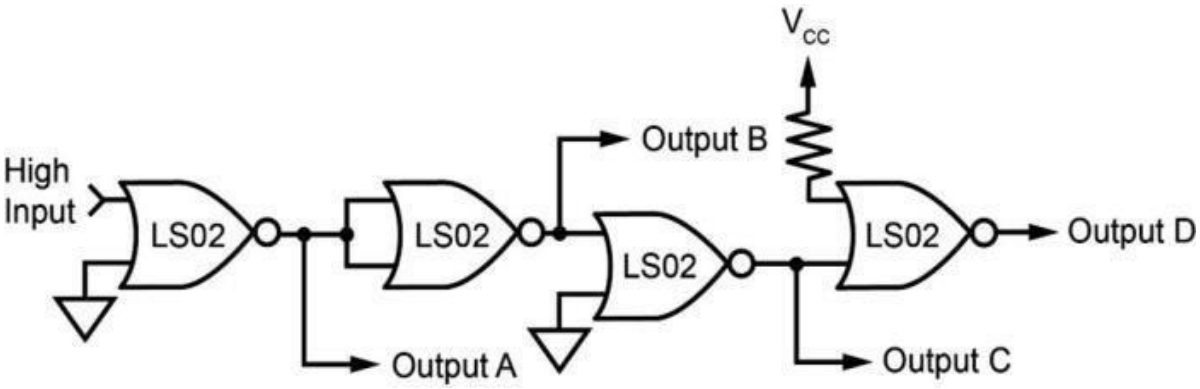


2. Place CM switch 12 in the ON position. The CM
    a. stops the gates from responding to input level changes at A.
    b. allows the gates to respond to input level changes at A.
    c. OR gate is enabled, but the NOR gate is disabled.
    d. NOR gate is enabled, but the OR gate is disabled.

3. The output of an OR gate is high
    a. all of the time.
    b. when any input is low.
    c. when any input is high.
    d. when all inputs are low.

4. The output of a NOR gate is low
    a. all of the time.
    b. when any input is low.
    c. when any input is high.
    d. when all inputs are low.

5. In the circuit shown, output levels A through D are, respectively,
    a. low, high, low, and low.
    b. low, high, low, and high.
    c. high, low, low, and low.
    d. disabled due to the circuit pull-up and common connections.



NOTE: Make sure all CMs are cleared (turned off) before proceeding to the next section.

Lab 2C: Logic Gates

➢ Objectives

- To learn the basic logic gates and verify selected circuits using digital circuit simulator called "**Deeds**" (Digital Electronics Education and Design Suite) simulator.
- You are required to work individually and answer the following questions.

➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

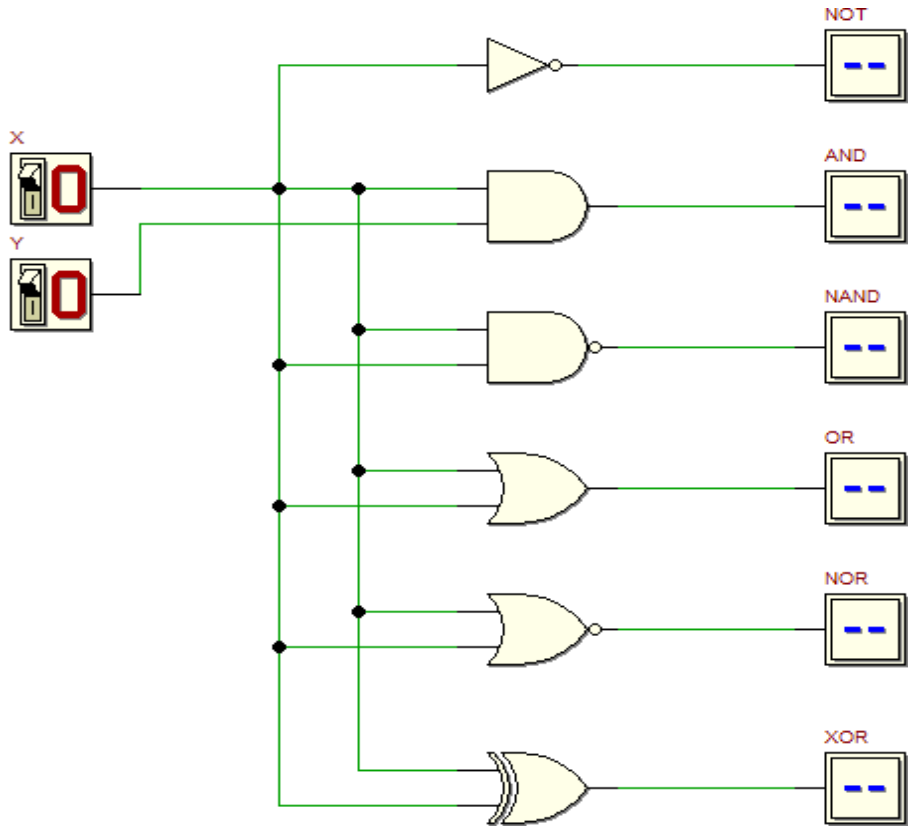
➢ Background :

Try out the following exercises (M. Mano, 5th Ed) before your lab:
2-2 (a, f), 2-4 (a, e), 2-5, 2-8, 2-10 , 2-12, 2-13, 2-14, 2-15, 2-18, 2-19, 2-24, 2-27

➢ Simulation:

Simulate the circuits of logic gates (NOT, AND, NAND, OR, NOR, and XOR) to verify their truth tables.

1- Use the simulator to draw the following circuit.

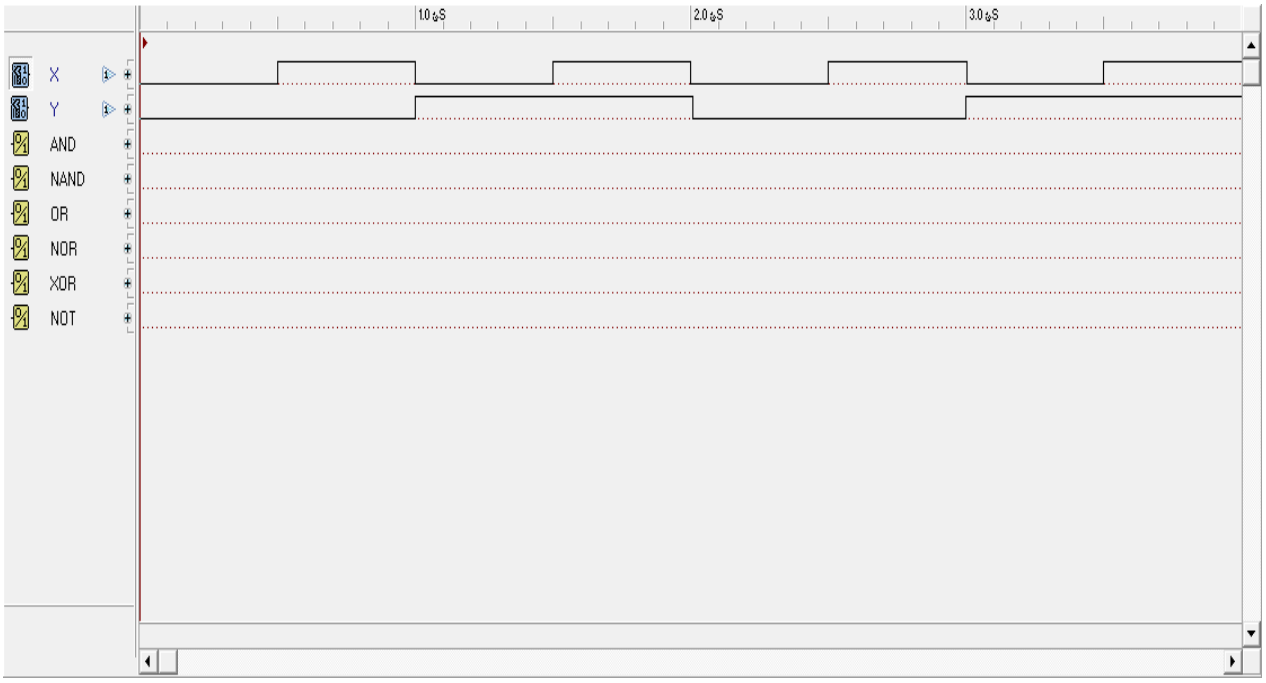


2- Start the **functional simulation (Interactive Animation)** of the network by clicking, on the **d-DcS toolbar**, the command  . Now the two input switches **X** and **Y** can be toggled and the gates' outputs NOT, AND, NAND, OR, NOR, and XOR will be changed accordingly.

3- According to the simulation results, fulfil the following truth table.

X	Y	NOT	AND	NAND	OR	NOR	XOR
0	0						
0	1						
1	0						
1	1						

4- Check the **timing simulation** of the circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window. You should define the values versus time of the two inputs, such as all the possible combinations of **X** and **Y** are tested as shown in the following figure.



➢ Reflection Questions

Student is required to submit the following:

- Answers to the exercises **2-14, 2-18, and 2-27** above.
- Deadline: at the beginning of the next Lab session.

Student answer to the reflection question:

Lab 3: Gate-Level Minimization

Objectives

- To learn the basics of Boolean Algebra and simplification using Boolean Algebra and Karnaugh map

Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

Background :

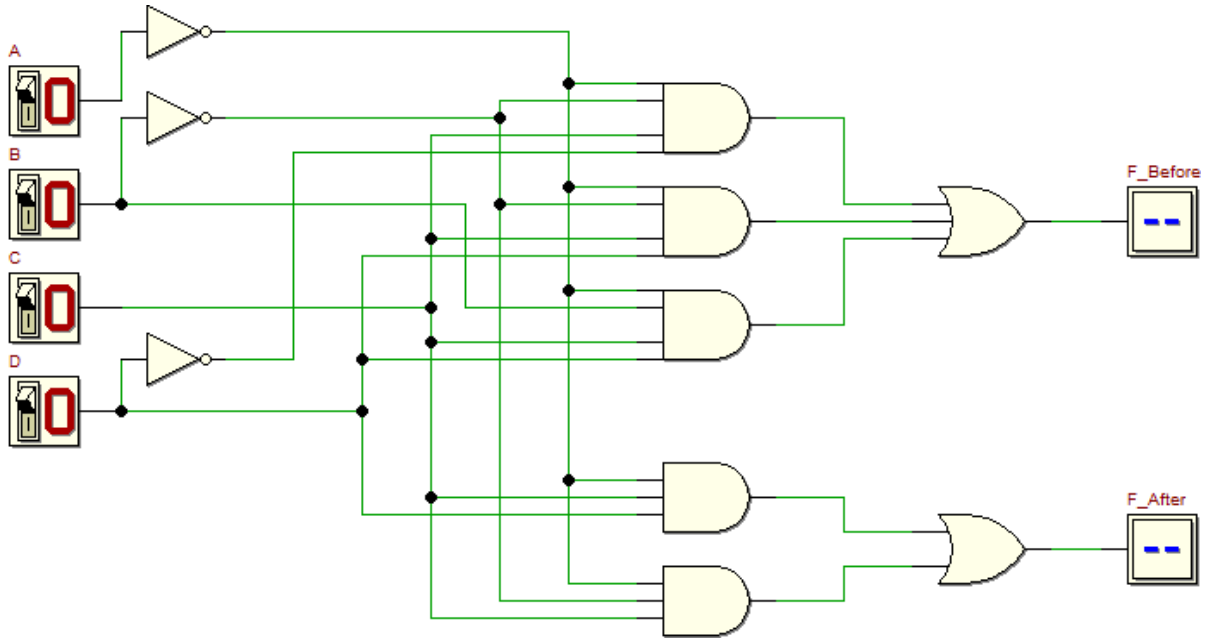
Try out the following exercises (M. Mano 5Ed) before your lab.
3-2 (c, d), 3-4 (a, b), 3-6 (a), 3-7, 3-9, 3-15 (a, b), 3-16 (a, d), 3-17, 3-18, 3-21.

Simulation

Simulate the logic diagram that implements the following function before and after the k-map reduction and fill-up the truth table for both circuits:

$$F(A, B, C, D) = \sum (2, 3, 7)$$

1- Use the simulator to draw the following circuit.

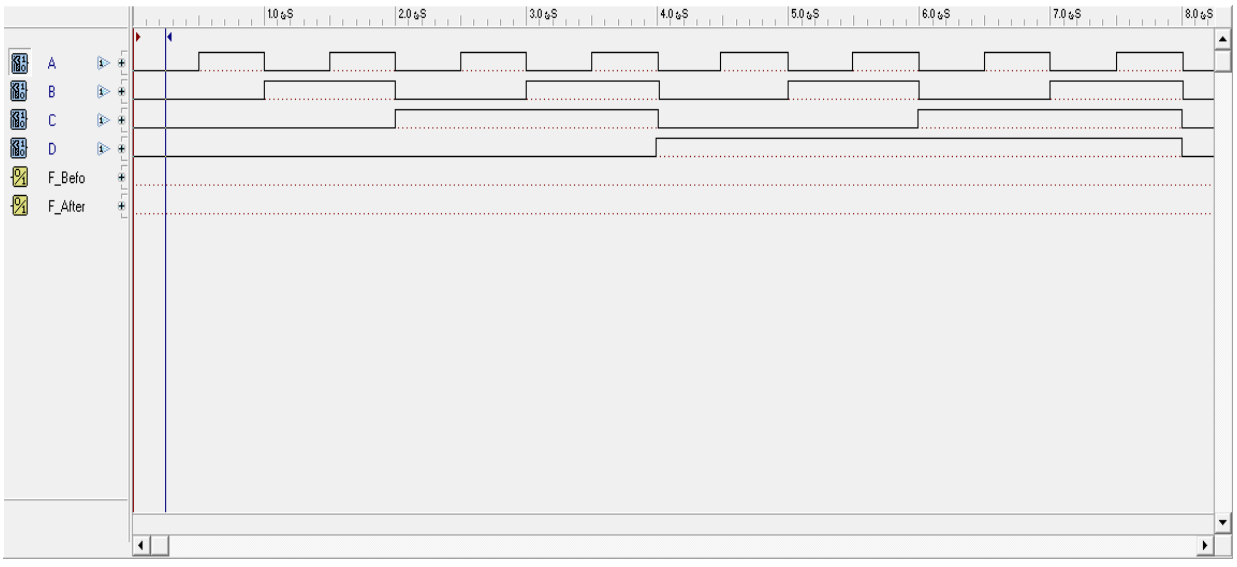


2- Start the **functional simulation (Interactive Animation)** of the circuit by clicking, on the **d-DcS toolbar**, the command  . Now the four input switches **A, B, C,** and **D** can be toggled and the outputs F_Before and F_After will be changed accordingly.

3- According to the simulation results, fulfil the following truth table. Compare the results before and after simulation.

X	Y	C	D	F_Before	F_After
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

4- Check the **timing simulation** of the circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window. You should define the values versus time of the two inputs, such as all the possible combinations of **A, B, C,** and **D** are tested as shown in the following figure. Also draw the corresponding outputs on the following figure.



➢ Reflection Questions

Student is required to submit the following:

- Answers to the exercises **3-4 (a, b) and 3-17** above.
- Deadline: at the beginning of the next Lab session.

Student answer to the reflection question:

Lab 4A: Fundamental Binary Addition

➢ OBJECTIVE

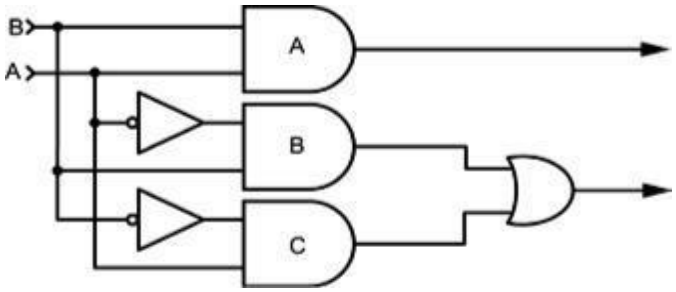
When you have completed this exercise, you will be able to predict the output of a 4-bit adder. You will verify your results by using a 4-bit adder to add two 4-bit words.

➢ REQUIREMENTS

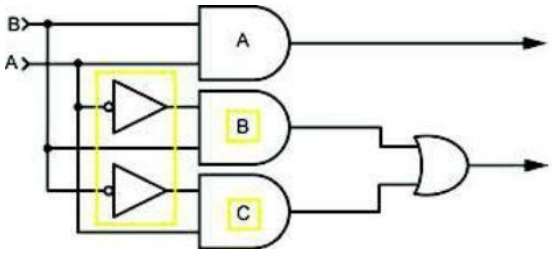
- DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
- PC or a Laptop computer

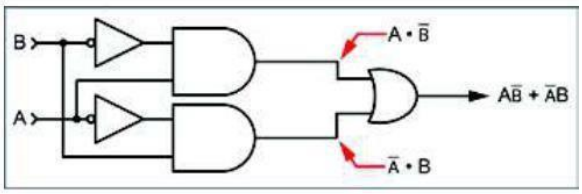
➢ DISCUSSION

The combinational logic of the gates shown illustrates the circuit of a single adder stage.

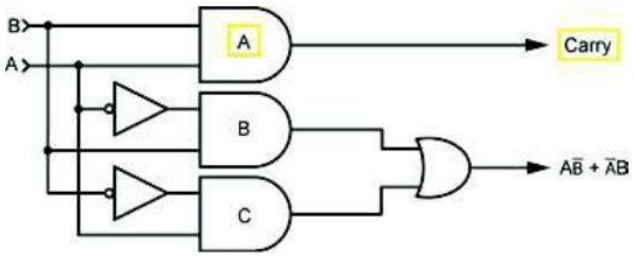


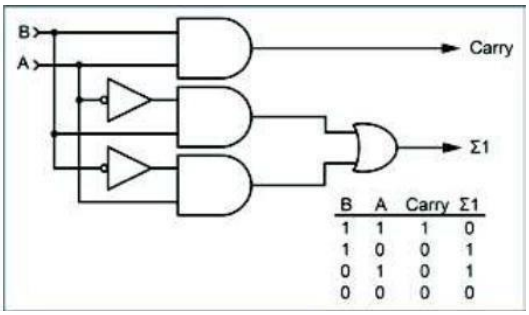
The circuit NOT gates ensure that gates B and C respond to unequal inputs.



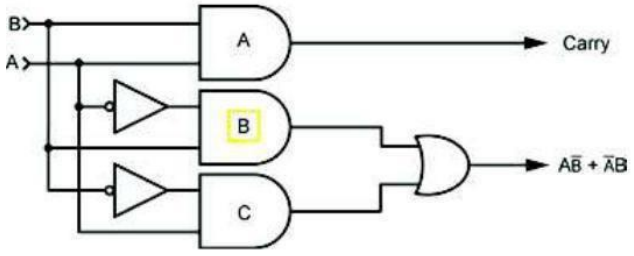


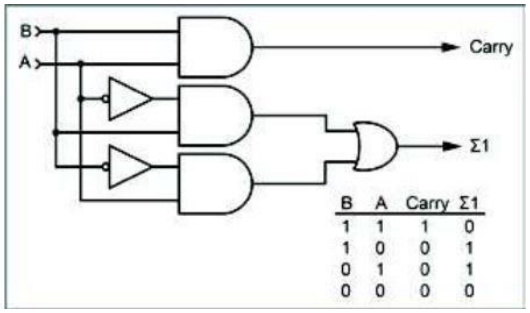
Gate A generates a 1 (carry detection) if A and B are both 1.



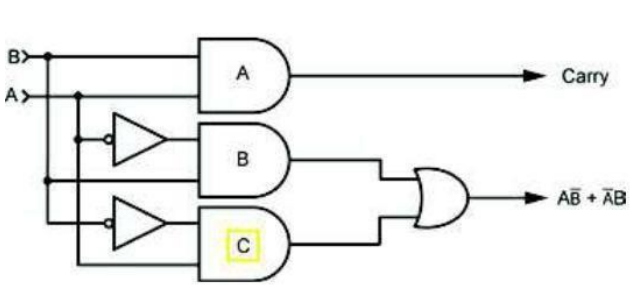


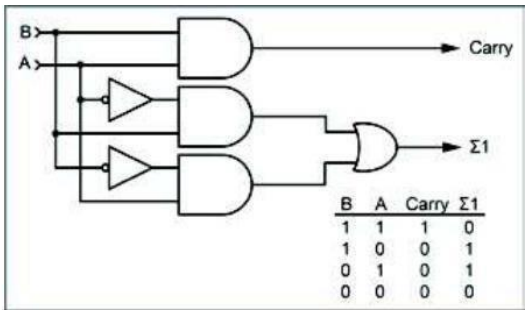
Gate B generates a 1 if A equals 0 and B equals 1.



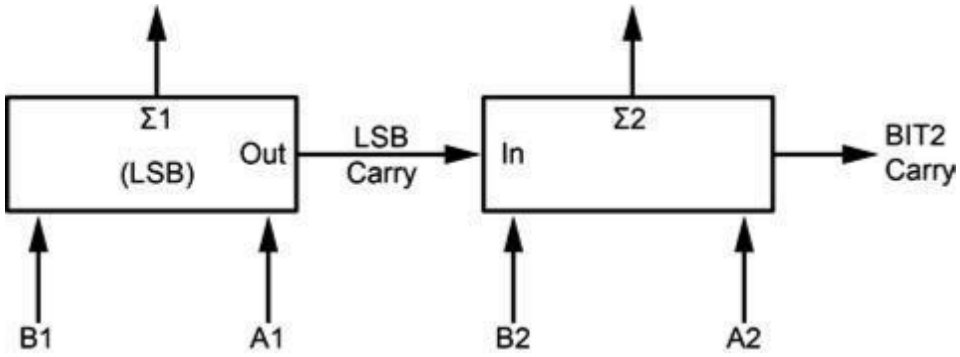


Gate C generates a 1 if A equals 1 and B equals 0.

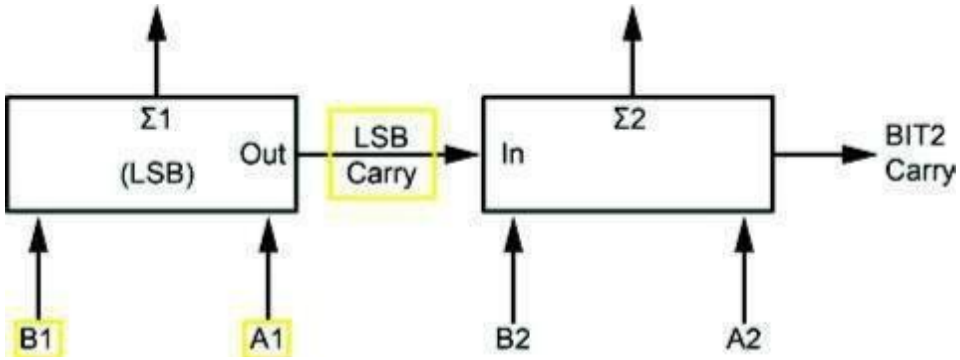




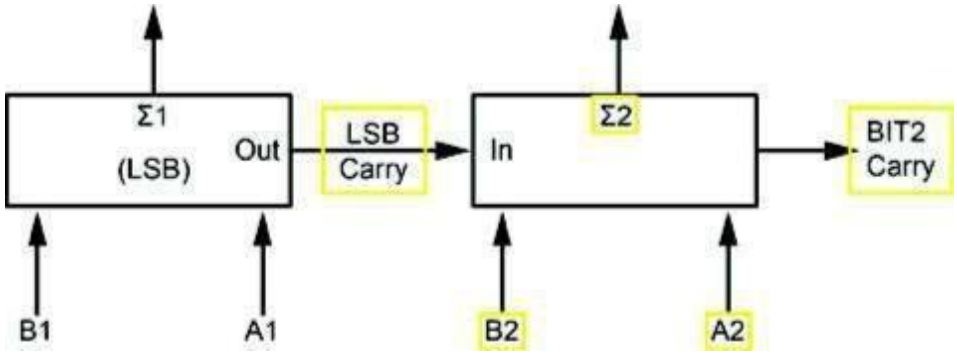
If two stages are cascaded, they have the elements of a two 2-bit word adder.



The LSB CARRY is 0 until A1 and B1 equal 1. Then, ∑1 is 0, and the LSB CARRY is 1.

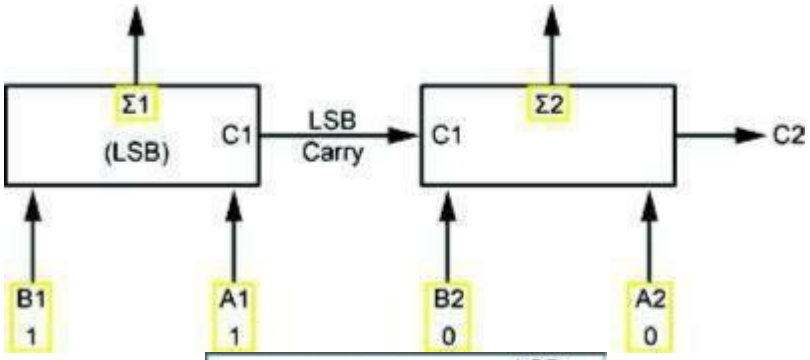


LSB CARRY OUT from the LSB stage serves as a CARRY IN to the next stage (∑2 = IN + B2 + A2). BIT2 CARRY is high if ∑2 > 1.



Q: Based on the data given, what is the circuit binary output?
NOTE: Your answer is in the form of MSB >>> LSB.

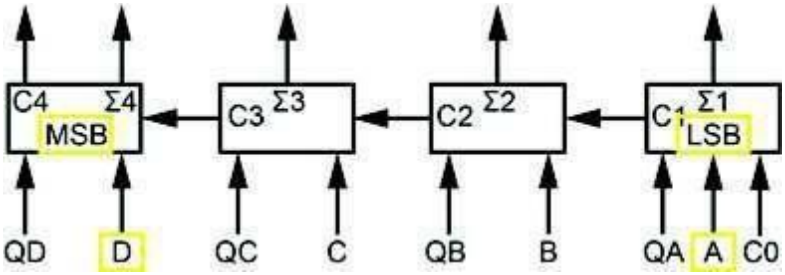
a. 11 b. 10 c. 01 d. 00



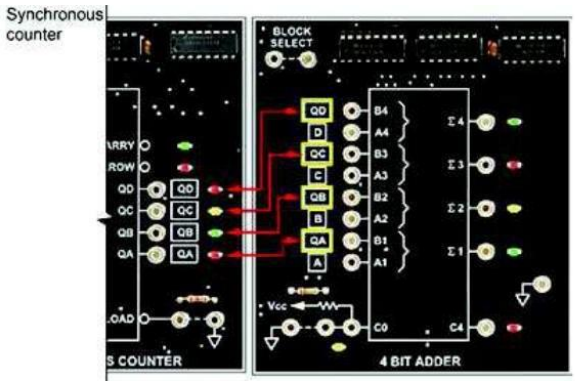
B1	A1	Σ1	LSB C1 Out
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

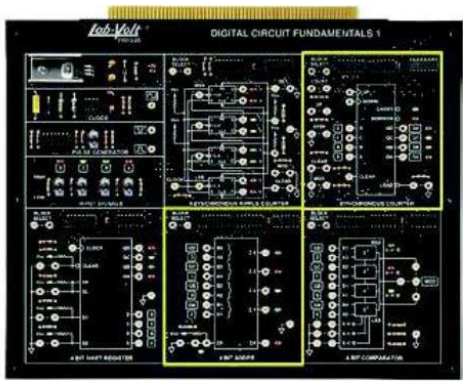
LSB C1 In	B2	A2	Σ2	BIT2 C2
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Stage A is the LSB stage of the adder. Stage D is the MSB stage.

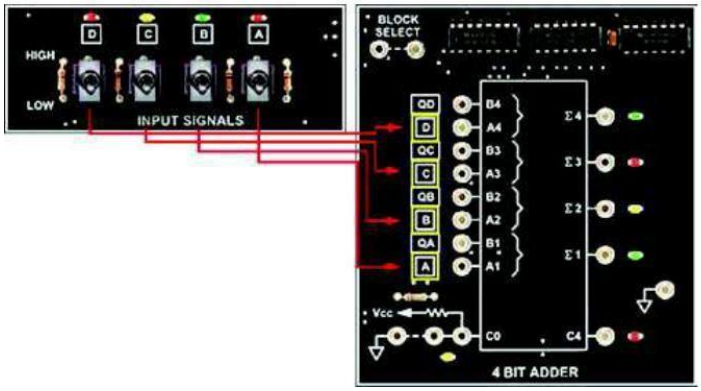


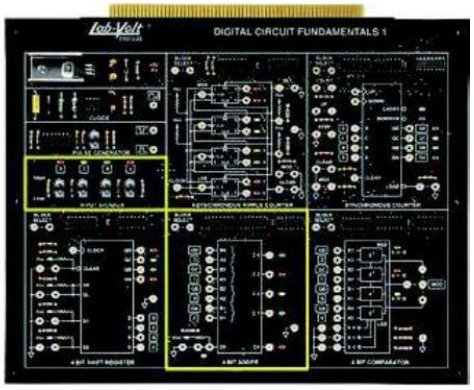
Outputs QD through QA of the SYNCHRONOUS COUNTER circuit block are used (hardwired) as inputs to the 4 BIT ADDER circuit block.



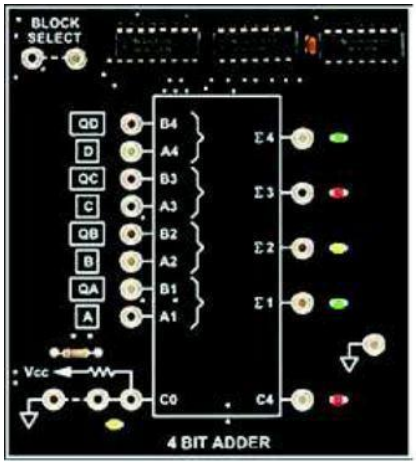


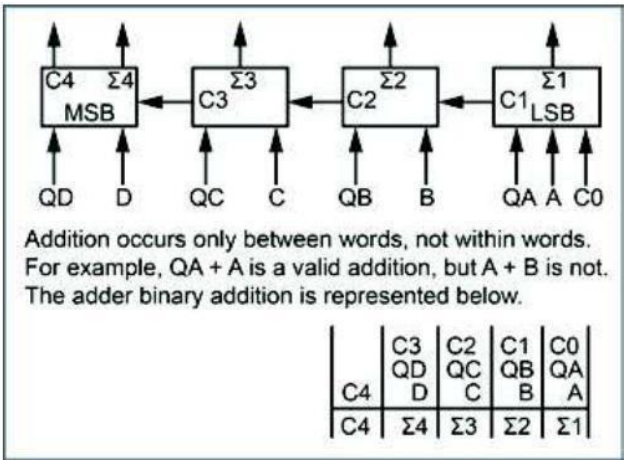
Inputs D through A of the 4 BIT ADDER circuit block are hardwired to toggle switches D through A of the INPUT SIGNALS circuit.





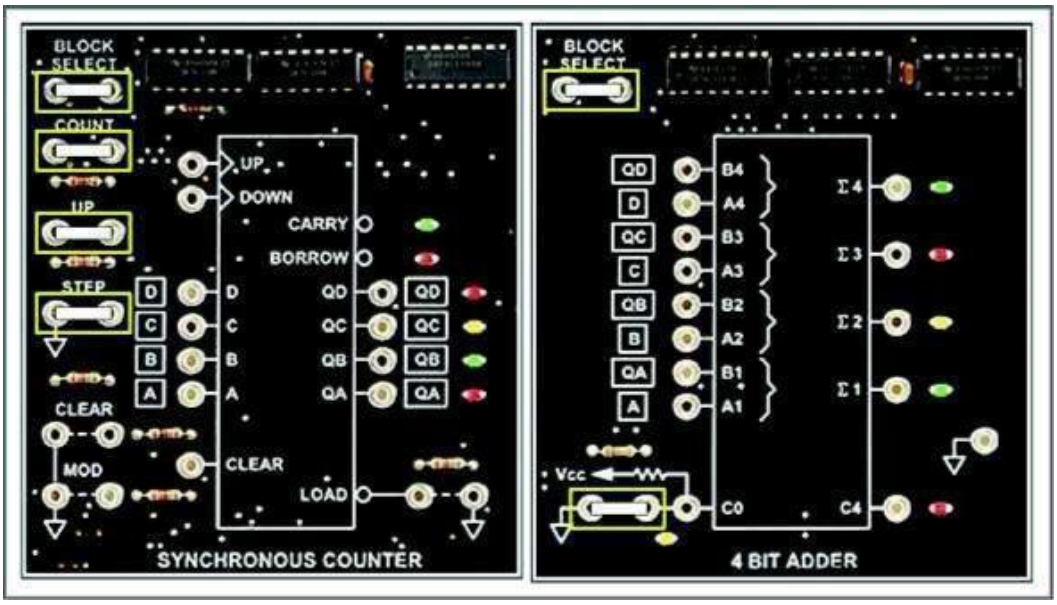
Inputs to any one stage are paired: A and QA, B and QB, C and QC, and D and QD.
A through D comprise one 4-bit word, and QA through QD comprise the second 4-bit word.
Addition occurs only between words, not within words.





- **PROCEDURE**

Locate the SYNCHRONOUS COUNTER and 4 BIT ADDER circuit blocks, and connect the circuit shown in the help window. The outputs of the counter are hardwired to inputs QD through QA of the adder.
NOTE: To clock the SYNCHRONOUS COUNTER circuit block, cycle the toggle switch on the PULSE GENERATOR circuit down then up.

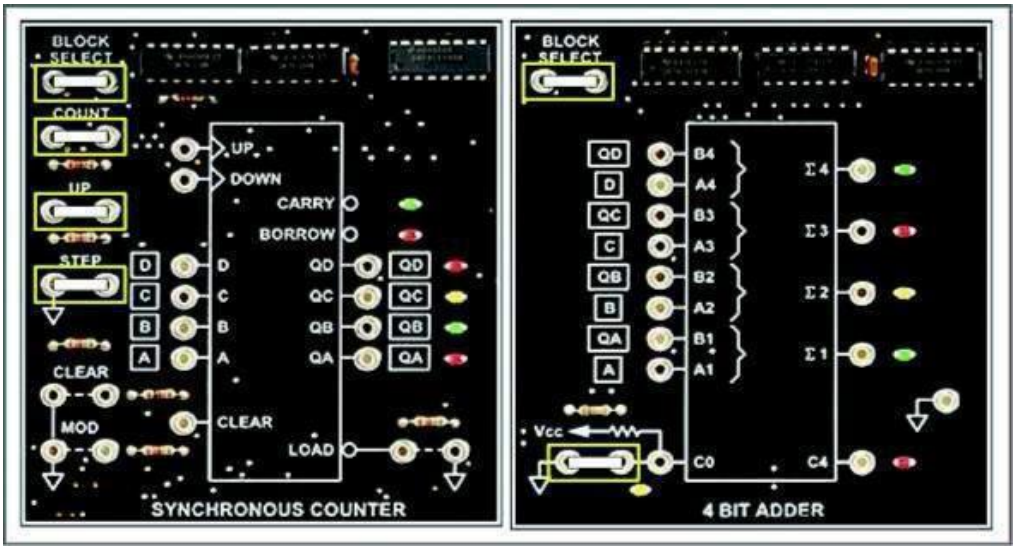


Reset the output of your SYNCHRONOUS COUNTER circuit block; momentarily enable the CLEAR function.
Place inputs D through A of your adder circuit to 0 (toggle switches D through A of the INPUT SIGNALS circuit down).

NOTE: The outputs of the INPUT SIGNALS circuit are hardwired to the adder's D through A inputs.
Based on the words A and B input of the adder, is the output value of 0000 correct?

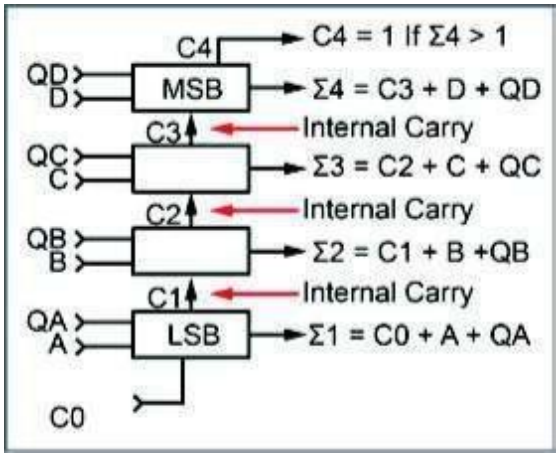
NOTE: The output LEDs of the SYNCHRONOUS COUNTER circuit block indicate the word Q input of the adder.

Q: The INPUT SIGNALS circuit LEDs indicate the bits A through D input of the adder.
a. yes b. no



Set INPUT SIGNAL A (bit A1) of your adder high (1).
Q: The output 1 is high because
a. 0 + 0 equals 102. b. 0 + 1 equals 12. c. it equals C0 + QA + A. d. Both b. and c.

Generate 1 CLOCK input for your synchronous counter. Do not change the adder A input level. Both A and QA of your adder circuit are high (1).
Q: Based on the adder output LEDs, an internal carry is
a. not generated. b. generated.

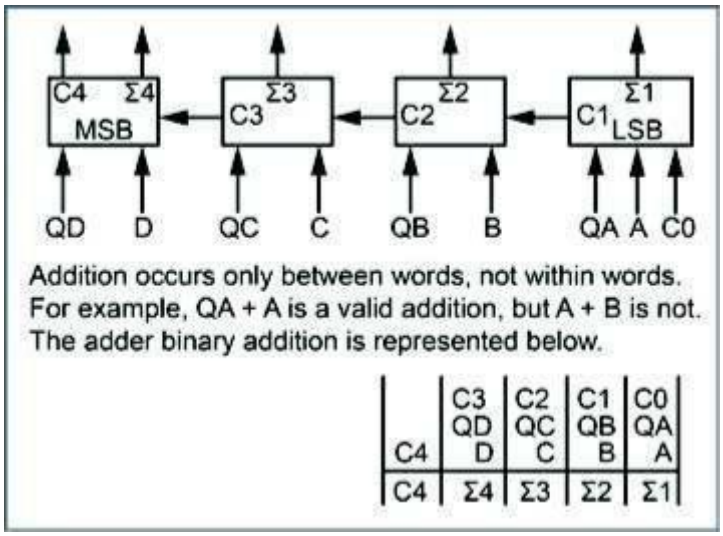


Clear, or reset, your synchronous counter (0000 output).

Set inputs A and B of your adder high.

Q: Why is output 3 low when A and B are both high?

NOTE: D through A respectively equal 0011, and QD through QA respectively equal 0000.
a. The adder cannot add A to B unless QB or QA has a nonzero input.
b. A and B represent bit inputs of the same word. Addition occurs between 4-bit word groups, not within a group.



Set QD through QA for 2_{10} and inputs D through A for 10_{10}.

Q: Based on your adder output, 210 + 1010, what is the binary and decimal output value?
a. 1100_2. b. 12_{10}. c. Both of the above. d. None of the above.

Decimal (Base 10) number	Binary (Base 2) number
16	1 0000
15	0 1111
14	1110
13	1101
12	1100
11	1011
10	1010
9	1001
8	1000
7	0111
6	0110
5	0101
4	0100
3	0011
2	0010
1	0001
0	0000

Binary weighted relationship

(2^3)	(2^2)	(2^1)	(2^0)	
8	4	2	1	
1	0	1	0	$= 10_{10}$ (8x1) + (4x0) + (2x1) + (1x0)
0	1	1	1	$= 7_{10}$ (8x0) + (4x1) + (2x1) + (1x1)
0	1	0	1	$= 5_{10}$ (8x0) + (4x1) + (2x0) + (1x1)

Activate the LOAD function of the SYNCHRONOUS COUNTER to set the counter output and adder input to 1111.
Set input A of your adder to 0001. Add 1111.

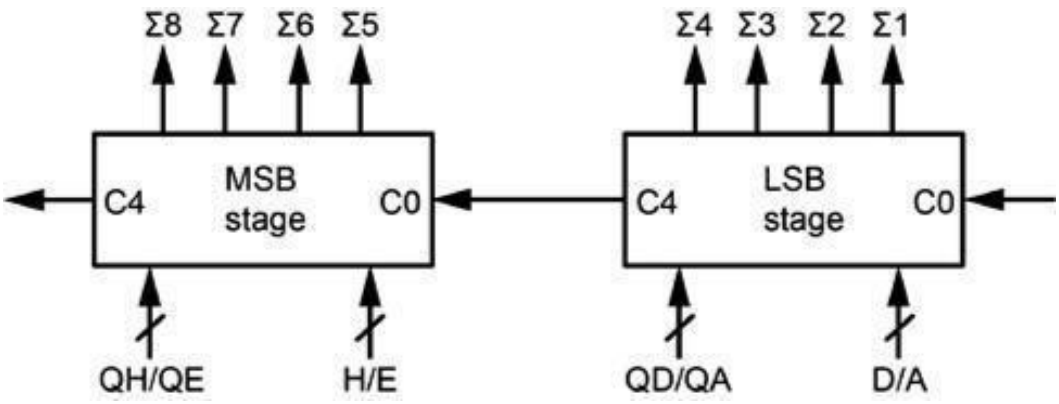
Q: Your adder indicates a sum of
a. 1111. b. 0000. c. (1)0000. d. (0)1111.

Remove the two-post connector from the C0 position (CARRY IN now equals 1).

Q: Based on the adder output, C0
a. is ignored. b. is added to the two 4-bit input words. c. automatically turns off C4. d. None of the above.

Can a 4-bit adder combine words having more than 4 bits?

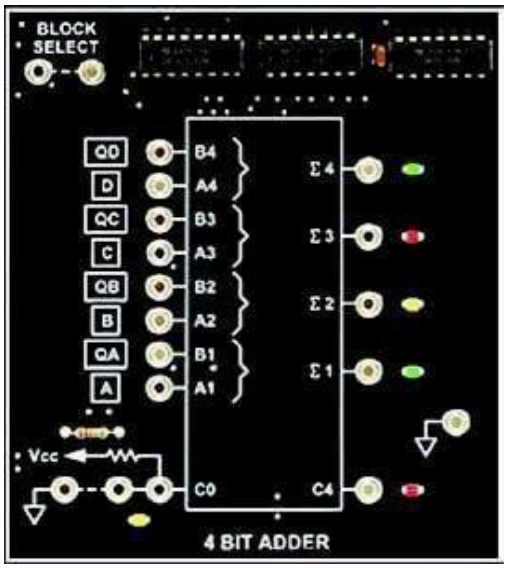
NOTE: Adder ICs can be cascaded.
a. yes b. no



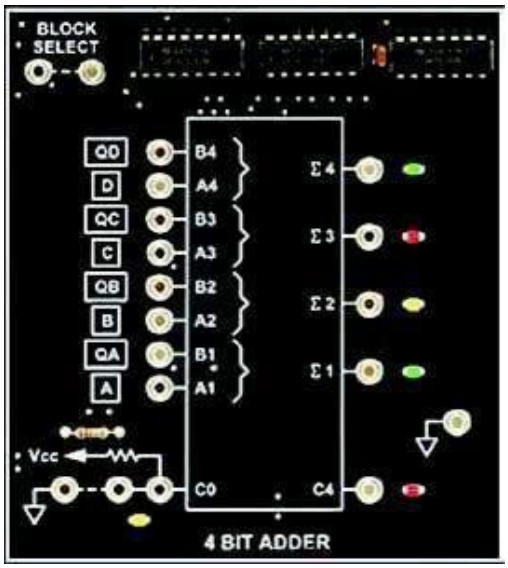
- **CONCLUSION**
  - The LS283 adder adds two 4-bit words.
  - A sum output is provided for each bit pair.

- **REVIEW QUESTIONS**

1. Each sum output of the adder is generated by
   a. all 4 bits of each word.
   b. its respective bit pair.
   c. adding 1 to the previous bit.
   d. None of the above



2. If adder inputs QA and QB are 1, and QC and QD are 0, what is the adder's output?
   a. 1100
   b. 0011 if the word A input is 0001
   c. 0100 if the word A input is 0001
   d. None of the above.



3. If word B equals 0100 and word A equals 1100, their sum is (1)0000. What is the decimal equivalent?

a. 8_{10}
b. 17_{10}
c. 15_{10}
d. 16_{10}

(2^4)	(2^3)	(2^2)	(2^1)	(2^0)
16	8	4	2	1
1	0	0	0	0

(16 x 1) + (8 x 0) + (4 x 0) + (2 x 0) + (1 x 0) = Base 10 equivalent of (1)0000

Lab 4B: Binary Addition and Carry

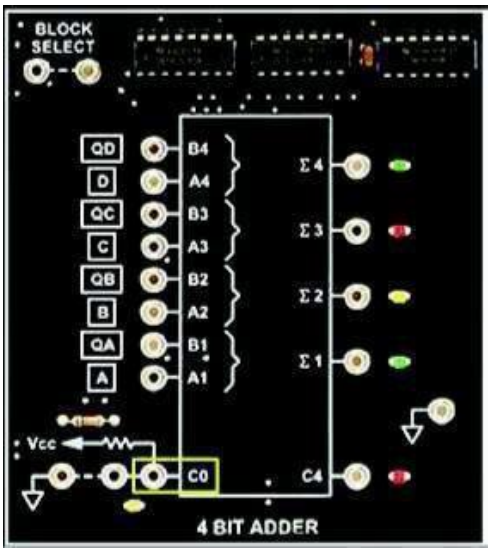
- **OBJECTIVE**

  When you have completed this exercise, you will be able to use the input C0 of your adder. You will verify your results by relating circuit waveforms to output binary sum values.

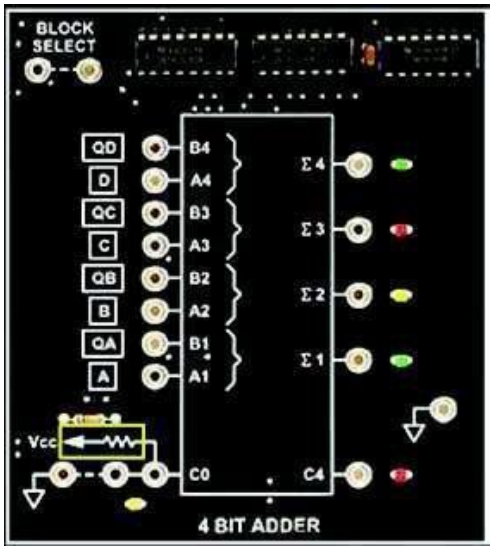
- **REQUIREMENTS**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - PC or a Laptop computer
  - An oscilloscope

- **EXERCISE DISCUSSION**

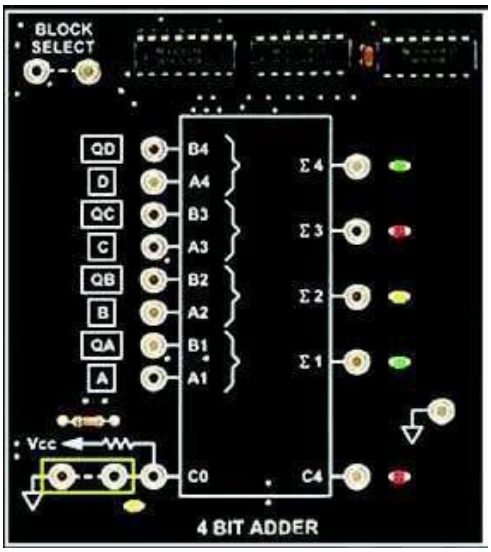
  Your adder has a C0 input, which represents a carry of 1 when it is activated (pulled to VCC).



When C0 pulled high, it has the same effect as adding 1 to the data being added.



C0 pulled to GND (common or 0) has no effect on data being added.



These examples show the effect of input C0 on the summed values of two 4-bit inputs (WORDS A and B).

Word B =	0000	0000	0001	0001	0001
Word A =	0000	0000	0000	0001	0001
C0 =	0000	0001	0000	0000	0001
Sum =	0000	0001	0001	0010	0011

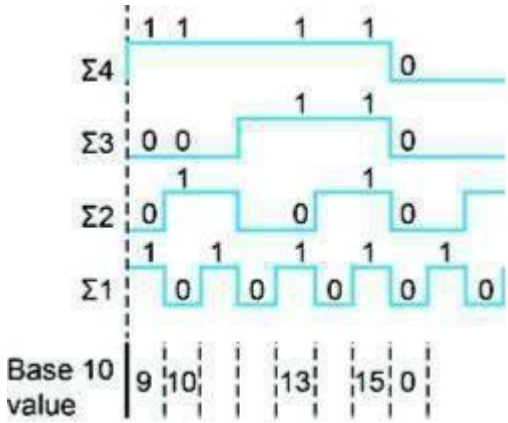
When input C0 is 1, the sum of WORDS A and B increases by 1 because input C0 ripples through the adder like any other bit input.

Word B =	0000	0000	0001	0001	0001
Word A =	0000	0000	0000	0001	0001
C0 =	0000	0001	0000	0000	0001
Sum =	0000	0001	0001	0010	0011

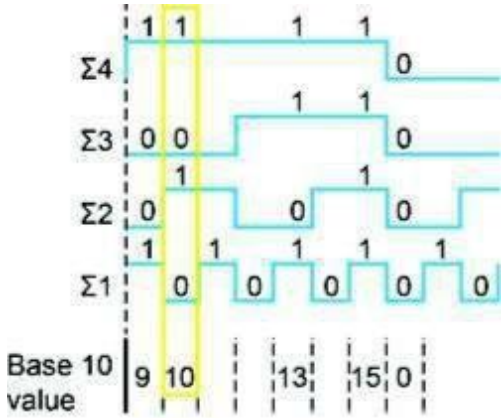
When input C0 is 0, there is no effect on the sum of WORDS A and B.

Word B =	0000	0000	0001	0001	0001
Word A =	0000	0000	0000	0001	0001
C0 =	0000	0001	0000	0000	0001
Sum =	0000	0001	0001	0010	0011

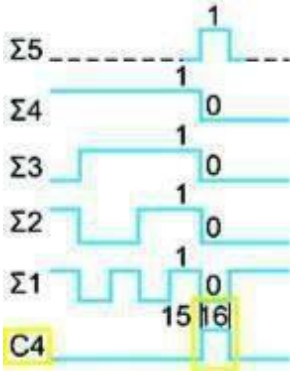
An oscilloscope can be used to monitor each output waveform of your adder. The relationship between the sum outputs determines the numeric value of the output.



For example, the output combination of 1010_2 equals 10_{10}. The adder outputs maintain a decimal-to-binary relationship.

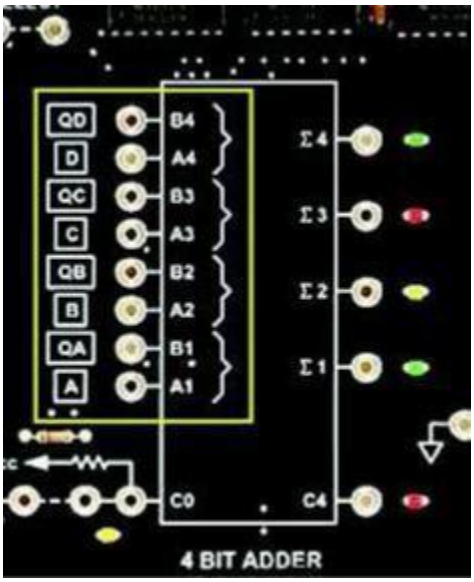


The C4 interval equals the time during which the adder output is greater than 15: (C4)0000.



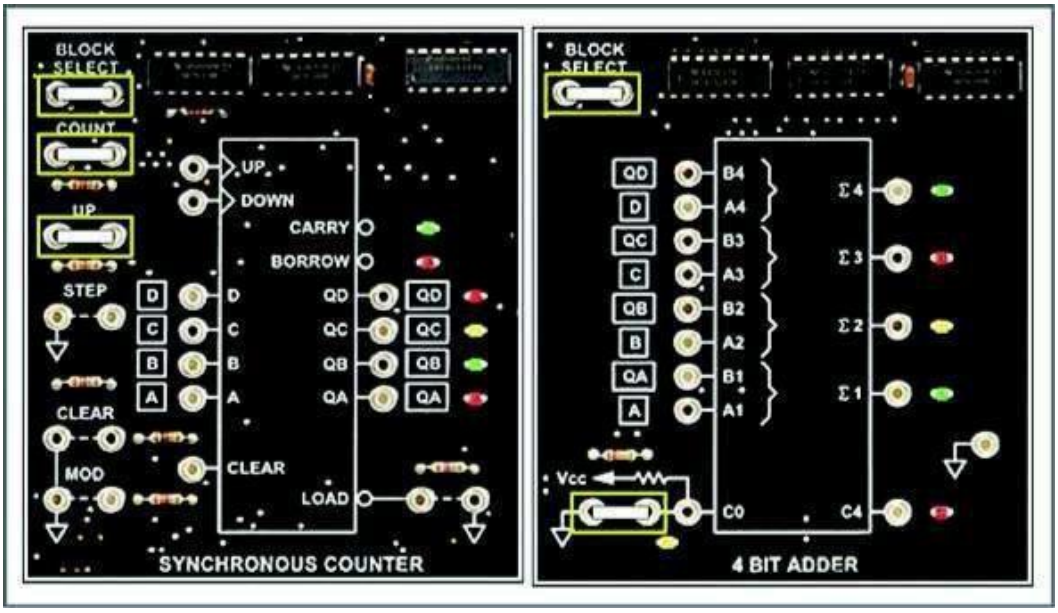
- **PROCEDURE**

In this procedure, adder inputs D through A are referred to as word A. Inputs QD through QA are referred to as word B. QD through QA are identical to B4 through B1 respectively (word B). D through A are identical to A4 through A1 respectively (word A).

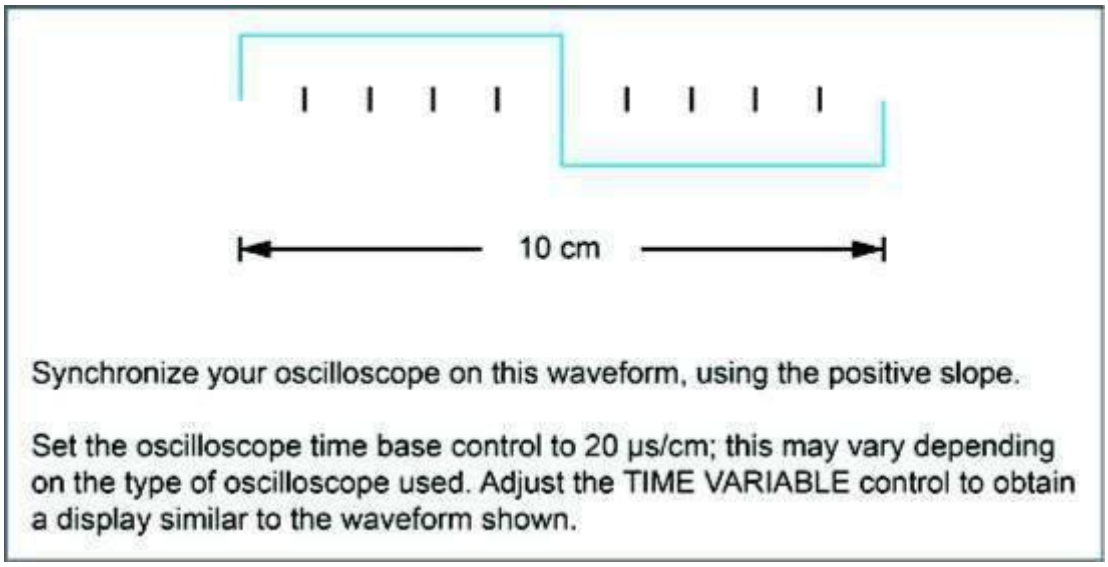


Locate the SYNCHRONOUS COUNTER and 4 BIT ADDER circuit blocks, and connect the circuit shown in the image below.

NOTE: The toggle switches of the INPUT SIGNALS circuit control inputs D through A on the 4 BIT ADDER circuit block. Inputs QD through QA are controlled by the SYNCHRONOUS COUNTER circuit block outputs.



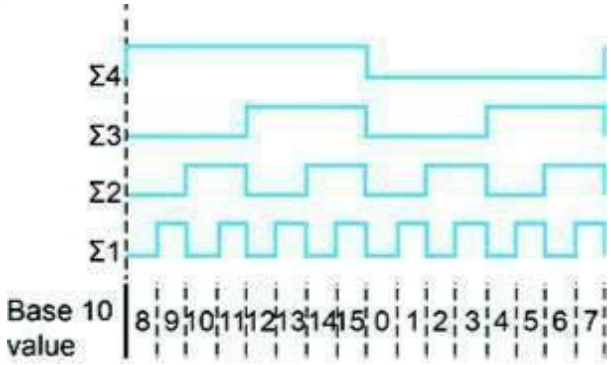
Set the word A input of your adder to 0000.
Connect oscilloscope channel 1 to the adder output test point. Display one cycle of the waveform over 10 cm.



Synchronize your oscilloscope on this waveform, using the positive slope.

Set the oscilloscope time base control to 20 μs/cm; this may vary depending on the type of oscilloscope used. Adjust the TIME VARIABLE control to obtain a display similar to the waveform shown.

Use oscilloscope channel 2 to monitor each sum output of your adder. You should observe a set of waveforms similar to the pattern shown.



Monitor adder output C4 on oscilloscope channel 2.

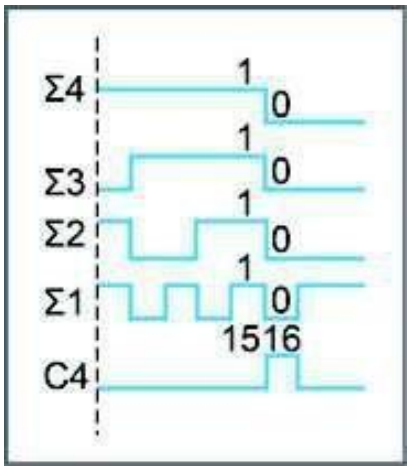
Q: Based on your observations, does the adder generate a carry output?

a. yes b. no

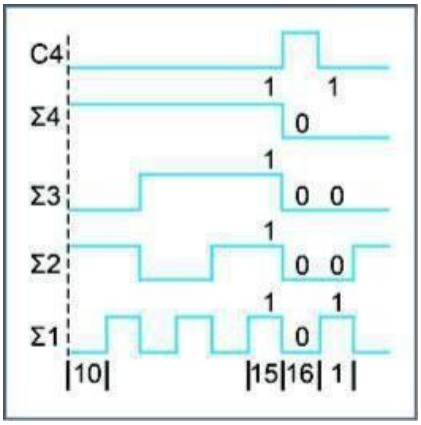
Set the word A input of your adder to 0001 (LSB = 1). Use oscilloscope channel 2 to observe the adder output waveforms (including C4).

Q: Based on your observations, what is the displayed output value just prior to the C4 time slot?

a. 1111 b. 1010 c. 0101 d. 0000



Q: What is the displayed value of the **6** outputs during the C4 time slot?
a. 1111 b. 1010 c. 0101 d. 0000



Set the word A input of your adder to 0000. Remove the two-post connector from input C0 of your adder circuit.

Q: Based on your oscilloscope waveforms, what is the effect of input C0?
a. C0 has no effect. b. C0 adds 1 to the counter value.
c. C0 cancels the CARRY OUT bit. d. C0 cancels the CARRY IN bit.

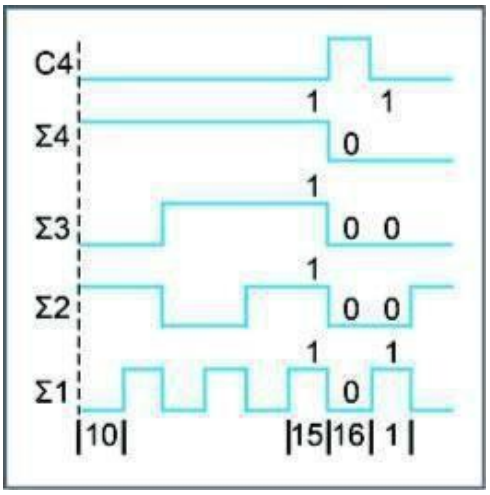
Set your oscilloscope TIME BASE control to 50, 64 (channel 1) and C4 (channel 2) on your oscilloscope.

NOTE: Switch to a calibrated time base. You may use other time base settings.

Make the adder's A input high, and note the duration (pulse width) of the adder's C4 output.
Q: The increase in the C4 time period (increasing pulse width) with respect to the output value of your adder indicates that the adder output value is increasingly
a. less than 15. b. greater than 15.

Set the word A input of your adder to 0001 (LSB = 1). Replace the two-post connector in the C0 position of your adder circuit.
Place CM switch 9 in the ON position to pull QD of the adder to VCC.
Set your oscilloscope TIME BASE control to 20. Use oscilloscope channel 2 to monitor the adder's **6** outputs (including C4).

Q: Based on your circuit waveforms, what is the numeric range of the adder output?
a. 0 through 15 b. 0 through 9 c. 9 through 15 d. 9 through 16



Q: How can you be certain that the total range of the adder is displayed on the oscilloscope?

a. You cannot be certain.

b. Ensure that the lowest or highest adder output is displayed twice during one sweep period of the oscilloscope.

c. re-adjust the oscilloscope settings

d. None of the above.

Q: Why is the adder output range restricted to a value between 9 and 16 (15 with a carry from C4)?
NOTE: Measure the word B input at the adder test points.

a.

b. Word B is offset to 1000 (minimum).

c. Both of the above.

d. None of the above.

Make sure all CMs are cleared (turned off) before proceeding to the next section.

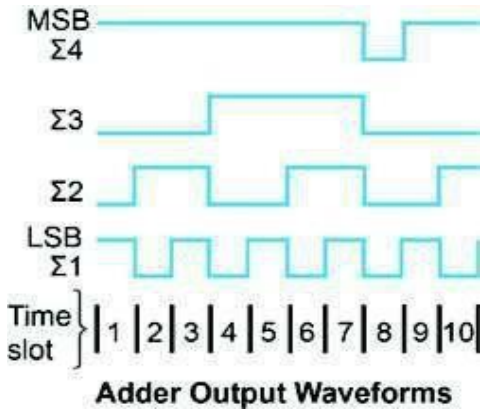
➢ CONCLUSION

- You can use the output waveforms of an adder to determine the output numeric value.
- If the adder generates a number greater than 15, output C4 is set high.
- If input C0 is high, the output increases by 1.

➢ REVIEW QUESTIONS

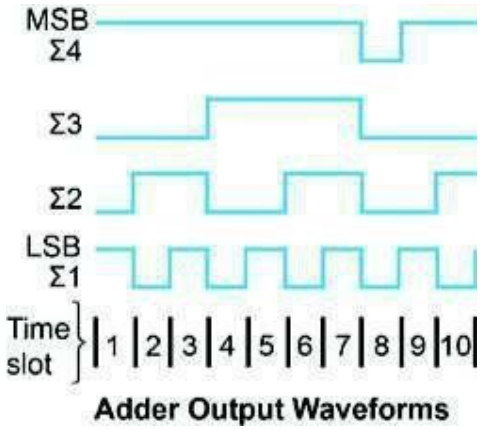
1. When C4 of your adder is activated, in which time slot should it appear?

a. 7 b. 8 c. Either of the above. d. None of the above.



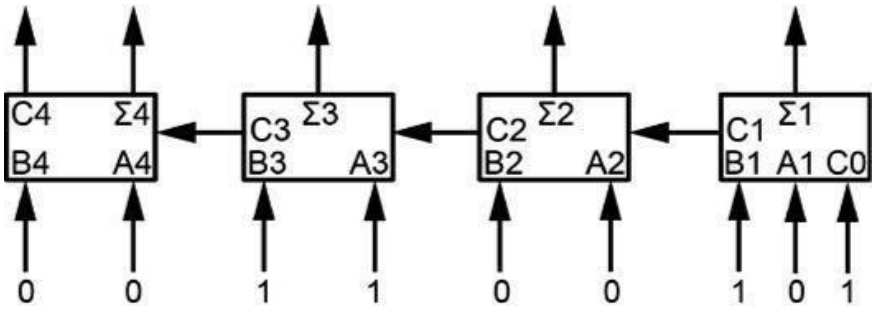
Adder Output Waveforms

2. Based on the output waveforms shown, the adder output
   a. value sequences are between 0 and 16.
   b. value must be offset to be correct.
   c. value equals the time slot number.
   d. sequence is 9 through 15, 0, 9, and 10.



Adder Output Waveforms

3. Based on the given information, what is the adder's output value?
   a. 1010 b. 1001 c. 0101 d. (1)1010



Lab 4C: Binary Comparisons

- **OBJECTIVE**

When you have completed this exercise, you will be able to perform comparisons of two 4-bit binary words. You will verify your comparisons on the 4 BIT COMPARATOR circuit block.

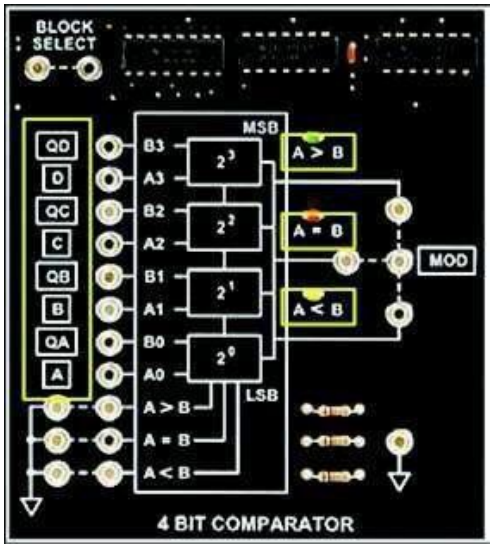
- **REQUIREMENTS**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - PC or a Laptop computer
  - An oscilloscope

- **EXERCISE DISCUSSION**

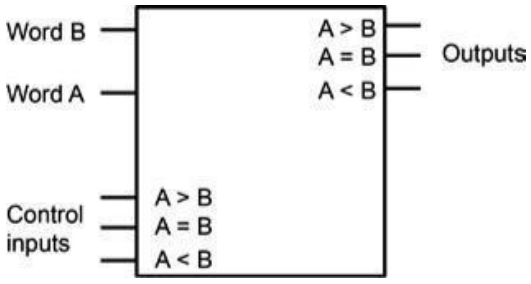
Toggle switches D through A on the INPUT SIGNALS circuit control inputs D through A on the 4 BIT COMPARATOR circuit block.

The QD through QA inputs of the 4-BIT COMPARATOR circuit block are hardwired to the SYNCHRONOUS COUNTER circuit block; therefore, these inputs require the operation of the counter.

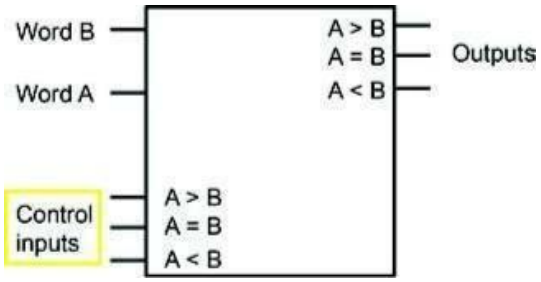
Your 4-bit comparator makes decisions about two 4-bit words. The result of the comparison is available at 3 outputs: A > B, A = B, and A < B.



Your comparator has two basic operating modes: words A and B equal and words A and B not equal.



The setting of the 3 input control lines (A > B, A = B, and A < B) determines the output code pattern generated for each mode.



The operating states and control codes for equal inputs are governed by the following truth table. When words A and B are equal, the cascade inputs control the levels at the comparator output.

Comparing Inputs				Cascade Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A = B	A < B	A > B	A = B	A < B
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	H	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	H

The operating states and control codes for unequal inputs are governed by the following truth table.

Comparing Inputs				Cascade Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A = B	A < B	A > B	A = B	A < B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	L	H
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	L	H

When words A and B are not equal, the cascade inputs do not affect comparator operation.

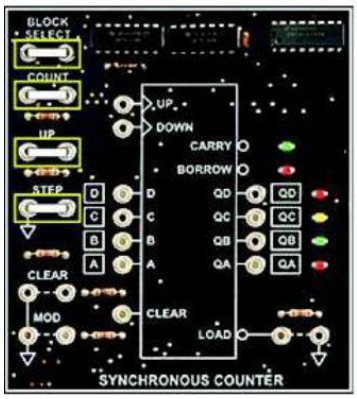
Comparing Inputs				Cascade Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A = B	A < B	A > B	A = B	A < B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	L	H
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	L	H

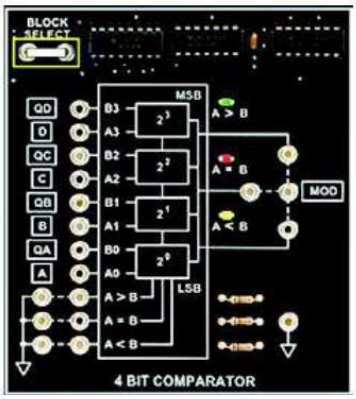
- **PROCEDURE**

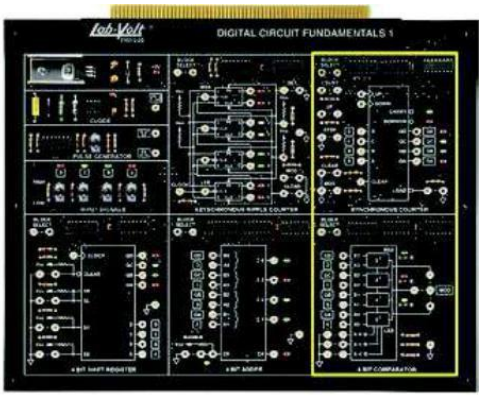
Place the toggle switches on the INPUT SIGNALS circuit in the DOWN position.
NOTE: The toggle switches control inputs A through D of the SYNCHRONOUS COUNTER and 4 BIT COMPARATOR circuit blocks.

Place the toggle switch on the PULSE GENERATOR circuit in the UP position.
NOTE: This toggle switch clocks the SYNCHRONOUS COUNTER circuit block.

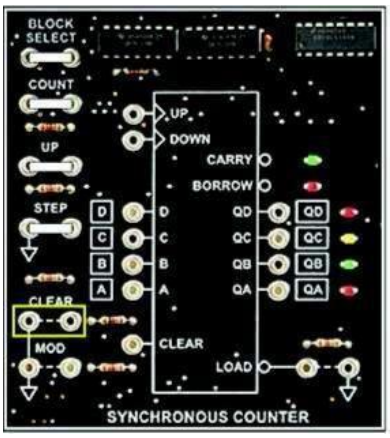
Locate the SYNCHRONOUS COUNTER and 4 BIT COMPARATOR circuit blocks, and connect the circuits as shown.

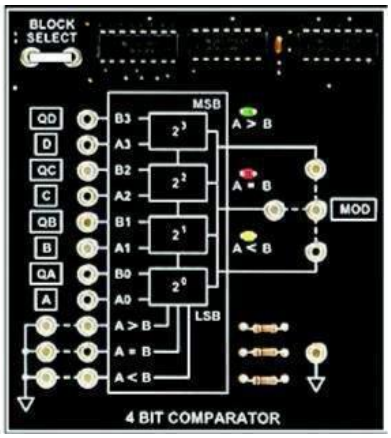






Use the CLEAR input of the counter to reset the counter outputs.





Q: Based on the output LEDs of the 4 BIT COMPARATOR circuit block, the word A and word B inputs are

a. equal. b. not equal.

NOTE: The cascade control inputs are pulled high. Therefore, the active A = B indication is high.

Comparing Inputs				Cascade Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A = B	A < B	A > B	A = B	A < B
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	H	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	H

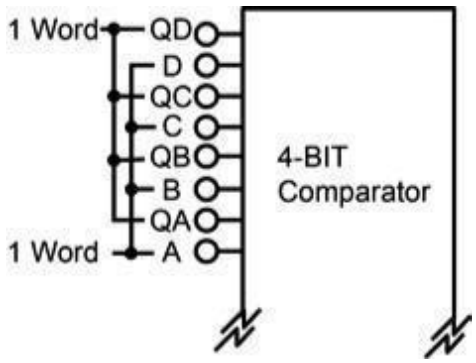
Operating states and control codes for **equal** inputs are governed by this truth table.

Q: How can you verify that the two word inputs are equal?

a. You cannot verify the comparator inputs.
b. Measure the comparator word A and word B inputs with an oscilloscope.
c. Remove all connectors to the 4 BIT COMPARATOR.

Use your oscilloscope to compare the two input words of the comparator.
Q: Are the bit pairs of each word identical?

a. yes b. no



Set input A of your comparator high.

Q: Based on the comparator output LEDs,
NOTE: WORD B = 0000. WORD A = 0001.

a. word B is greater than word A.
b. word B and word A are equal.
c. word B is less than word A.

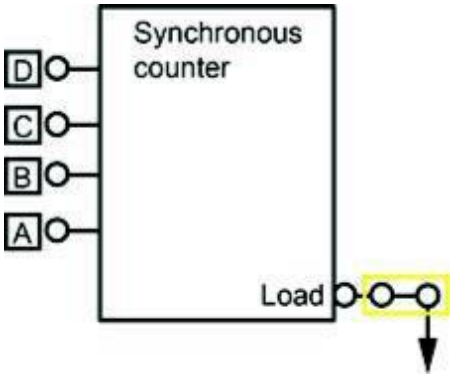
On your 4 BIT COMPARATOR circuit block, measure A (A0) and QA (B0).

Q: Based on your observations, can the comparator determine the relationship between two words if only one bit pair is not equal?

a. yes b. no

Use the parallel load function of your counter to set word B of your comparator to $A (1010).
NOTE: Place INPUT SIGNALS circuit toggle switches D through A at high, low, high, and low, respectively.

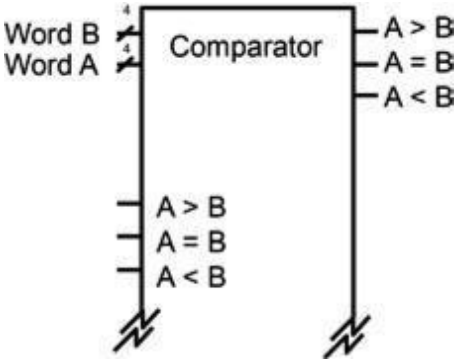
Then momentarily activate the counter LOAD input.



Because words A and B are equal, the A = B output LED of the comparator should be on.
NOTE: The D through A toggle switches are hardwired to the SYNCHRONOUS COUNTER and 4 BIT COMPARATOR circuit blocks.
When A was less than B, the A < B LED was on.

Q: For equal word inputs, which comparator inputs determine the active state (high or low) of the comparator outputs?

a. word A b. word B c. None of the above



Make words A and B of the comparator equal. Any equal values will do.

Use two-post connectors on the comparator control inputs to set the input states indicated by the table below, and note the comparator outputs for each row of the table.

Control Inputs		
A > B	A = B	A < B
L	H	L
H	L	H
L	L	L

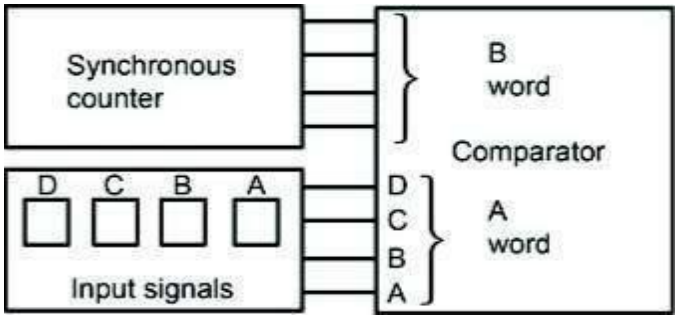
Q: Based on your results,

a. the comparator outputs exactly match the levels of the programming inputs.
b. the A = B output level matches the level of the A = B programming input.
c. no direct relationship exists between the programming inputs and the comparator outputs.

Comparing Inputs				Cascade Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A = B	A < B	A > B	A = B	A < B
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	H	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	H

Operating states and control codes for **equal** inputs are governed by this truth table.

Remove all two-post connectors from the control inputs of your comparator circuit.



Set both word B and word A to 1000 to initiate an A = B output. Use the word A controls to generate words of 1100, 1010, and 1001. Observe the comparator output for each word pattern.

Q: Based on your observations, does the comparator ignore all equal bit patterns and make a decision based only on unequal bits?

a. yes b. no

This table shows the individual bit groups to compare.

Word B Word A	1000 1100	1000 1010	1000 1001
Result	A > B	A > B	A > B

Make sure that all two-post connectors are removed from the programming, or control, inputs of the comparator.

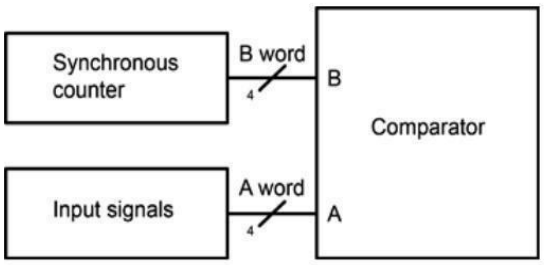
Q: If you repeat the comparing operation but alter word B instead of word A, could you expect the same output?

a. yes b. no

Set both word B and word A to 1000 to initiate an A = B output. Use the word B counter to generate words of 1100, 1010, and 1001. Observe the comparator output for each word pattern.

Q: Based on your A < B indication, comparisons are with respect to word

a. A b. B



This table shows individual word groups to compare.

Word B Word A	1100 1000	1010 1000	1001 1000
Result	A < B	A < B	A < B

On the SYNCHRONOUS COUNTER circuit block, use the UP control to decrement or increment the count.

➢ CONCLUSION

- A 4-bit comparator can make a decision about two 4-bit words.
- A comparator can generate A < B, A = B, and A > B indications about two 4-bit words.
- The active output indication (high or low) of a comparator is controlled by the A < B, A = B, and A > B inputs of the device.
- A comparator makes a decision between two words based on bit pairs that are not equal.
- The comparator you used in this exercise makes a decision with respect to the word A input: A < B, A = B, A > B.
- You can predict the output results of a comparison by performing a manual bit-by-bit comparison of the two words.

➢ REVIEW QUESTIONS

1. Word A equals 1000, and word B equals 0111. What does a comparison of the two words indicate?

a. A > B b. A = B c. A < B d. B > A

2. Word A equals 0111, and word B equals 1000. What does a comparison of the two words indicate?

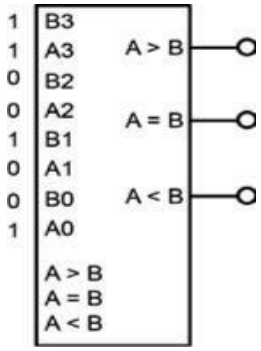
a. A > B b. A = B c. A < B d. B < A

3. If the input words to the comparator are equal, is it possible to have all low outputs (all LEDs off)?

a. No, this is not possible.
b. Yes, provided that the A = B input is pulled to GND.
c. Yes, but only when BLOCK SELECT is not activated.
d. No, unless the word inputs are complementary.

4. Word A equals 1001, and word B equals 1010. Your comparator decides that A is less than B because

a. of the LSB pair (bit pair 0).
b. of bit pair 1.



Lab 4D: Functions of Combinational Logic

➢ Objectives:

- To learn basic adders, parallel binary adders, ripple carry and look-ahead carry adders, and comparators.
- You are required to work individually and answer the following questions.

➢ Requirements:

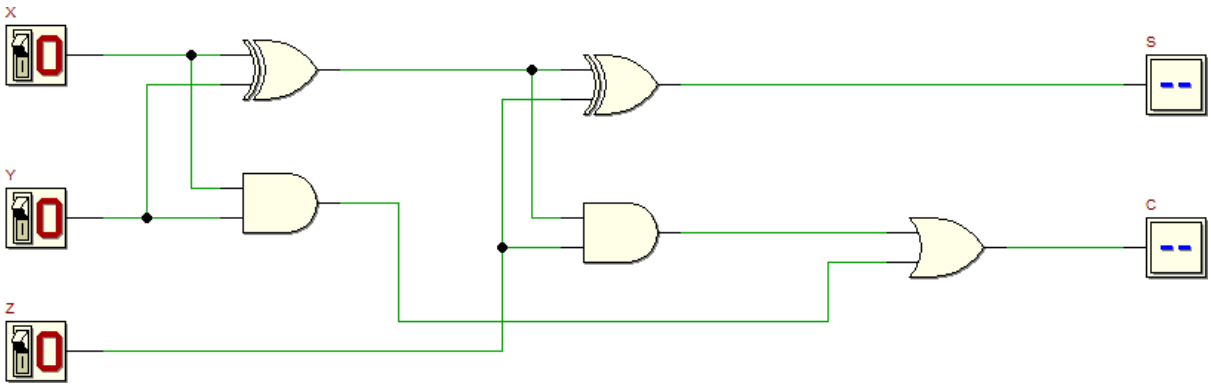
- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

➢ Background:

Try out the following exercises before your lab: 4.1(a,b), 4.2, 4.4(a), 4.5, 4.6(a), and 4.7

➢ Simulation:

1- Use the simulator to draw the logic circuit of the full-adder shown in the following figure.

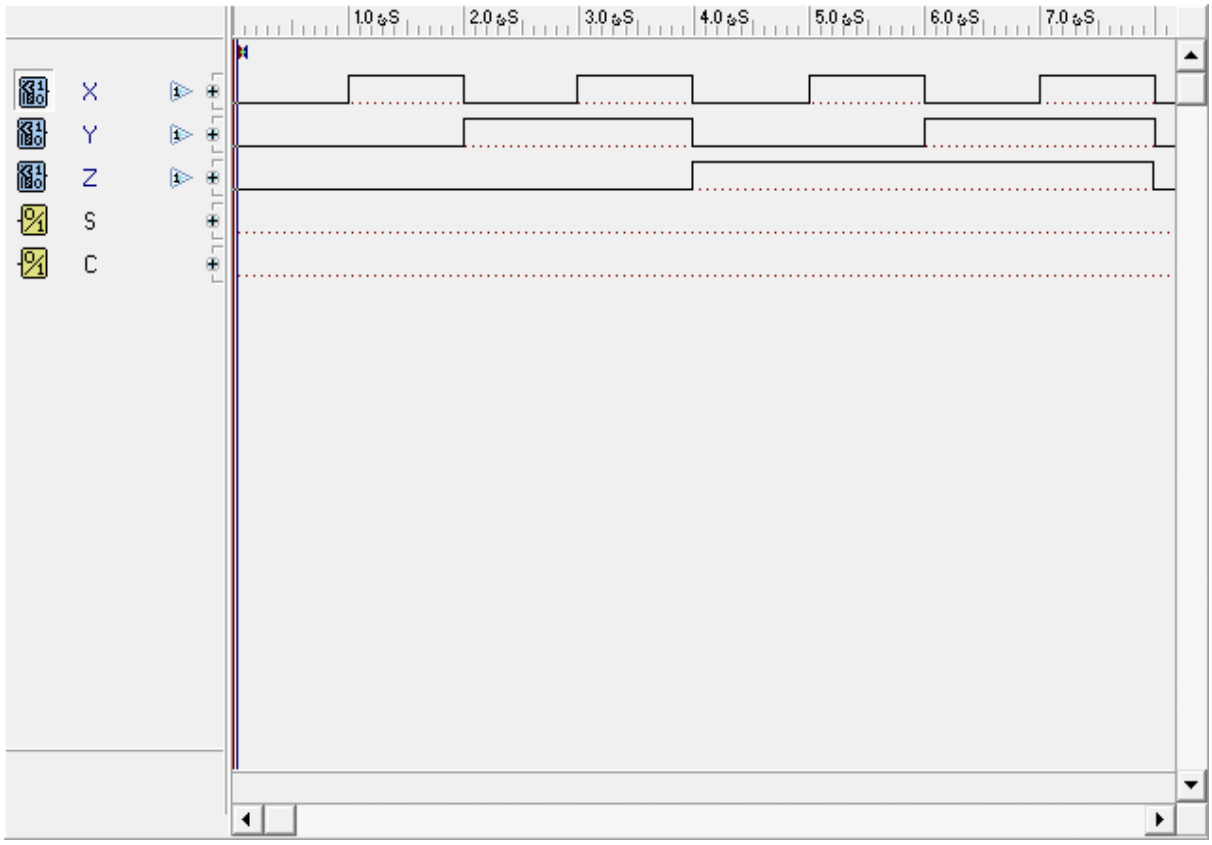


2- Start the **functional simulation (Interactive Animation)** of the circuit by clicking, on the **d-DcS toolbar**, the command  . Now the three input switches **X, Y,** and **Z** can be toggled and the outputs S (sum) and C (carry) will be changed accordingly.

3- According to the simulation results, fulfil the following truth table. Compare the results before and after simulation.

X	Y	Z	S	C
0	0	0		
0	0	0		
0	1	1		
0	1	1		
1	0	0		
1	0	0		
1	1	1		
1	1	1		

4- Check the **timing simulation** of the circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window. You should define the values versus time of the three inputs, such as all the possible combinations of **X, Y,** and **Z** are tested. Also draw the output resulted from the **timing simulation** on the on the following figure.



Reflection Question:

Student is required to submit the following:

- Answers to the exercises **4.7** above.
- Deadline: at the beginning of the next Lab session.

Student answer to the reflection question:

Lab 4E: Other Functions of Combinational Logic

➢ Objectives

- To learn the different combinational logic circuits such as decoders/encoders, code converters, multiplexers/demultiplexers and parity generators/checkers.
- You are required to work individually and answer the following questions.

➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

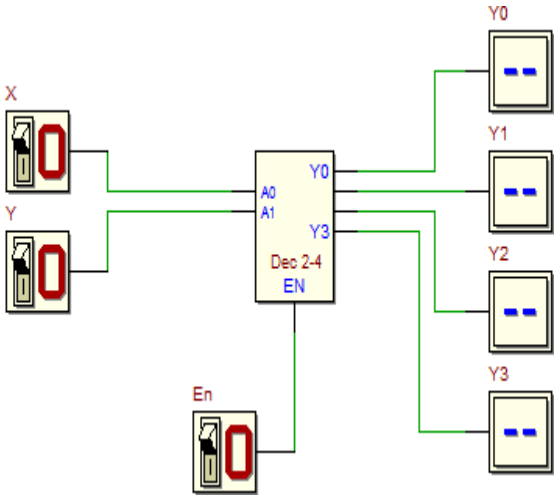
➢ Background:

Try out the following exercises before your lab:
4.22, 4.23, 4.24, 4.27, 4.28(a), 4.31, 4.33, and 4.35.

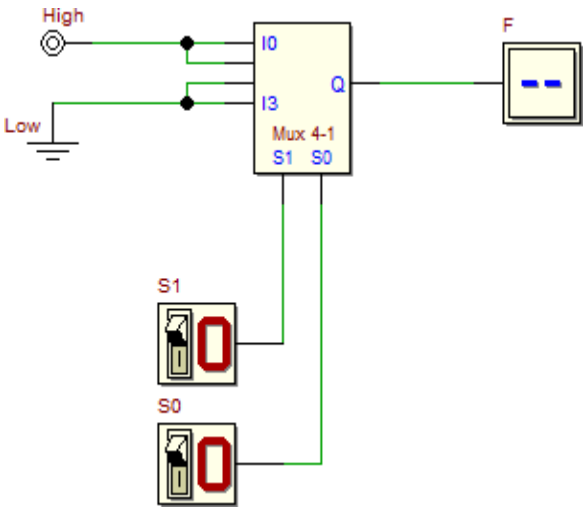
➢ Simulation:

1- Use the simulator to draw each of the following logic circuits in a separate file:

a. A 2-to-4-line decoder with enable input.
b. A 4-to-1-line multiplexer.



a) 2-to-4 Decoder



b) 4-to-1 Multiplexer

2- Start the **functional simulation (Interactive Animation)** of each circuit by clicking, on the **d-DcS toolbar**, the command  . Now the input switches of each circuit can be toggled and the corresponding outputs will be changed accordingly.

3- According to the simulation results of each circuit, fulfil each of the truth tables corresponding to each logic circuit.

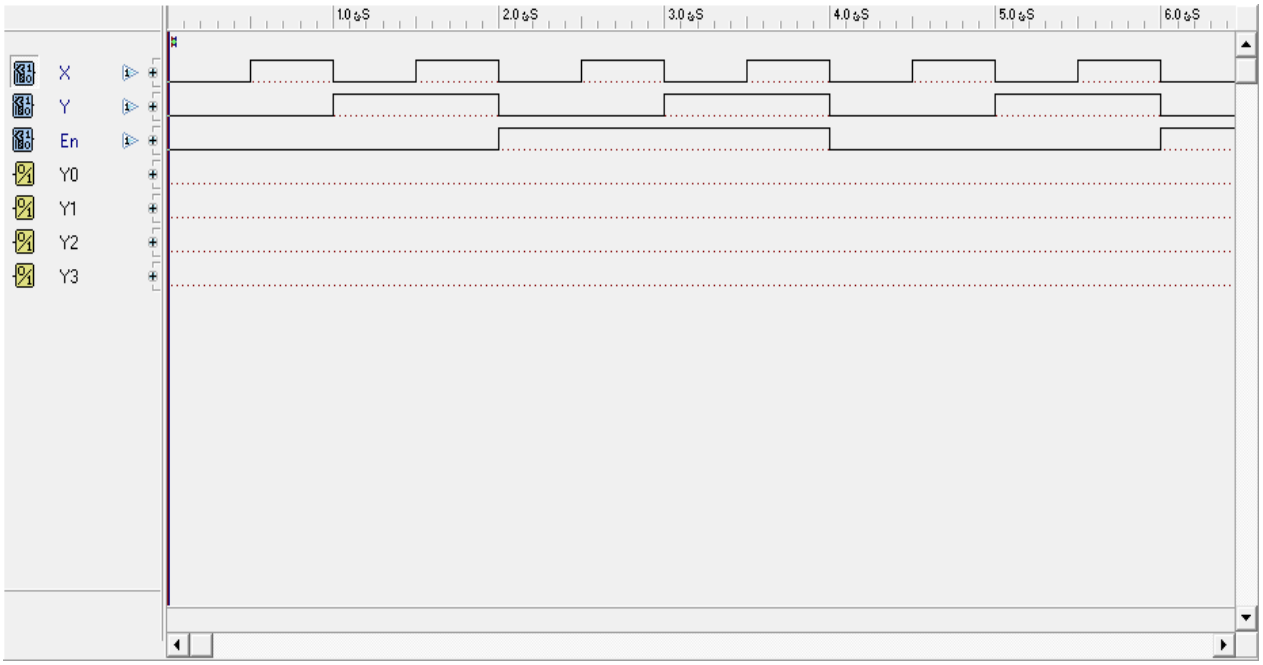
a) Decoder Truth Table

En	X	Y	Y_0	Y_1	Y_2	Y_3
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

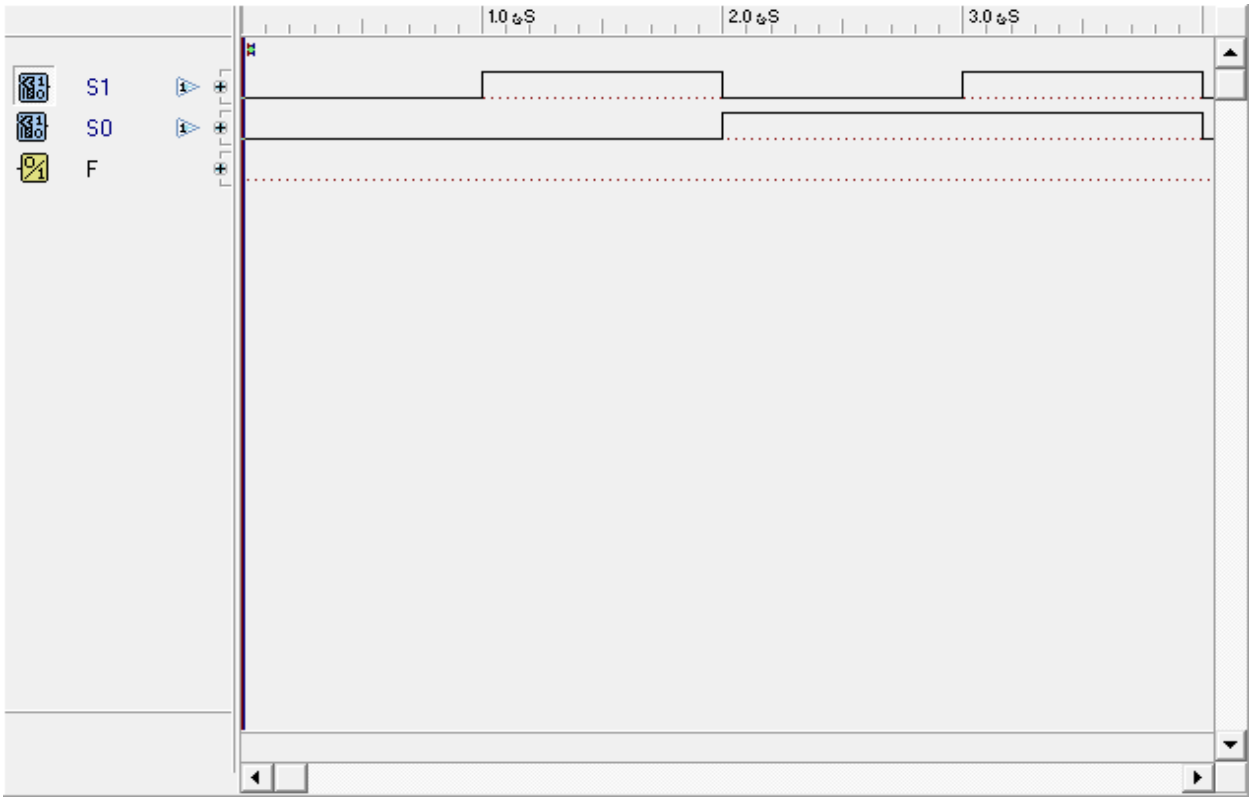
b) Multiplexer Truth Table

S_0	S_1	F
0	0	
0	1	
1	0	
1	1	

4- Check the **timing simulation** of each logic circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window. You should define the values versus time of the inputs such as all the possible input combinations are tested. Also draw the output resulted from each **timing simulation** on the corresponding figure of the following figures.



a) Decoder timing diagram



b) Multiplexer timing diagram

- **Reflection Questions:** Student is required to submit the following:
  - Answers to the exercises 4.33 and 4.35 above.
  - Deadline: The beginning of the next Lab session.

Student answer to the reflection question(if any)

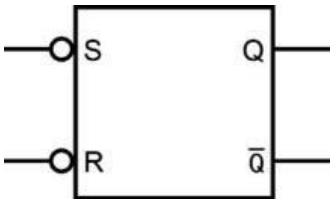
Lab 5A: Set-Reset Flip-Flop

- **OBJECTIVE**

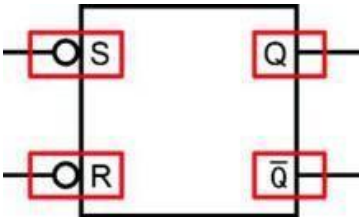
When you have completed this exercise, you will be able to demonstrate the operating characteristics of an SR flip flop and gain experience in using an Oscilloscope.

- **REQUIREMENTS**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - PC or a Laptop computer.
  - An oscilloscope

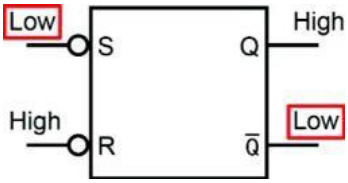
- **EXERCISE DISCUSSION**



There are two inputs, S (SET) and R (RESET), and two complementary outputs, Q and Q!.

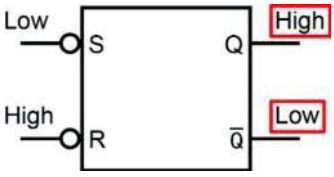


A logic low at input S combined with a logic high at R sets the Q output to logic high and the Q! output to logic low.

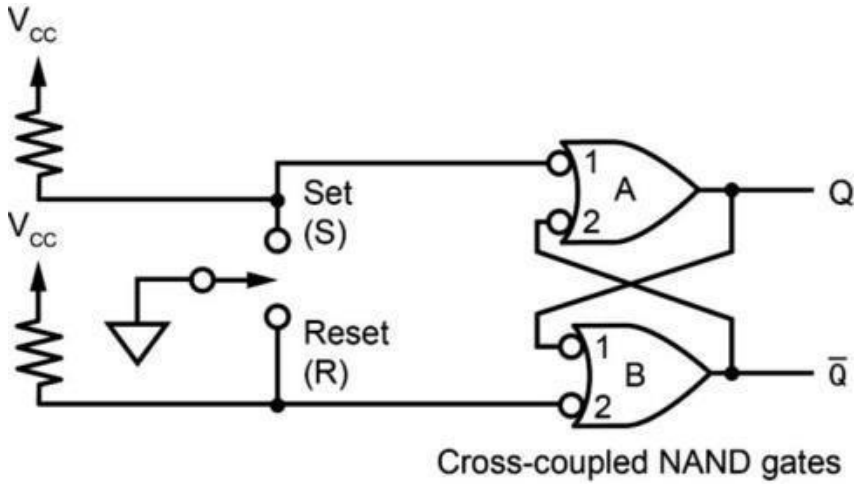


The Q output state is logic high and Q! is low.
Q: What will cause Q to go low and Q! to go high?

a. changing the S input to logic high
b. changing the R input to logic low and the S input to logic high
c. changing the R input to logic low
d. All of the above.

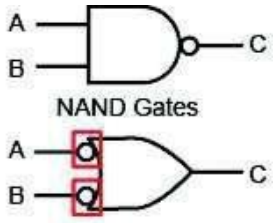


The following diagram shows two cross-coupled and inverted-input OR gates (similar effect to using two NAND gates) used within the SR flip-flop.



Cross-coupled NAND gates

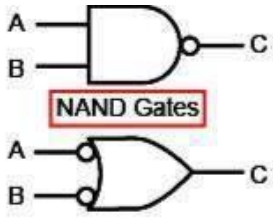
An OR gate with negated inputs has the same output states as a NAND gate.



A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

Truth table

Both symbols represent the same NAND gate circuit.

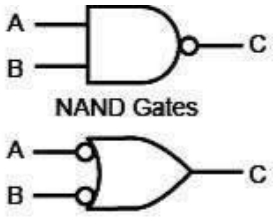


A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

Truth table

If the two inputs of a NAND gate represented by an OR gate with negated inputs are high and low, the output is

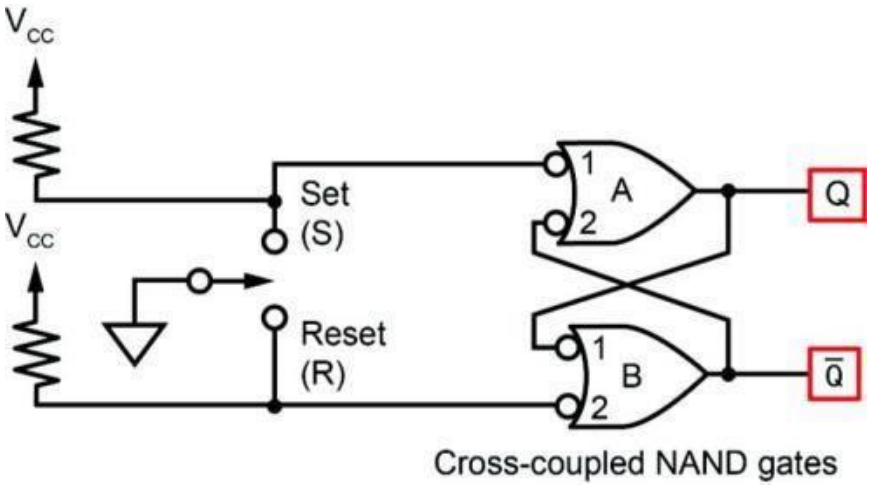
a. low. b. high.



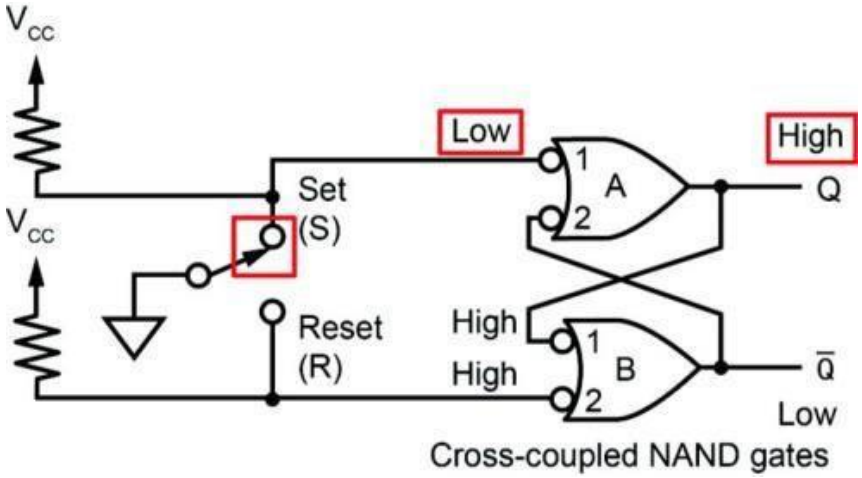
A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

Truth table

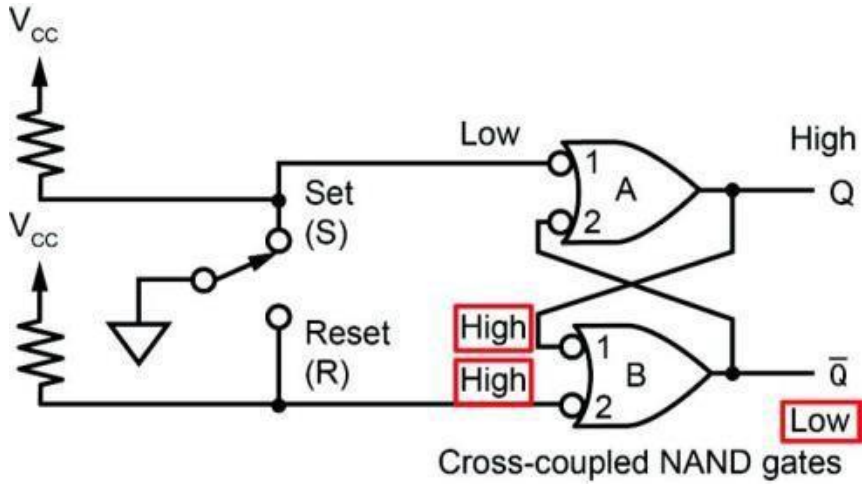
The following example relates to the cross-coupled NAND gates diagram shown:



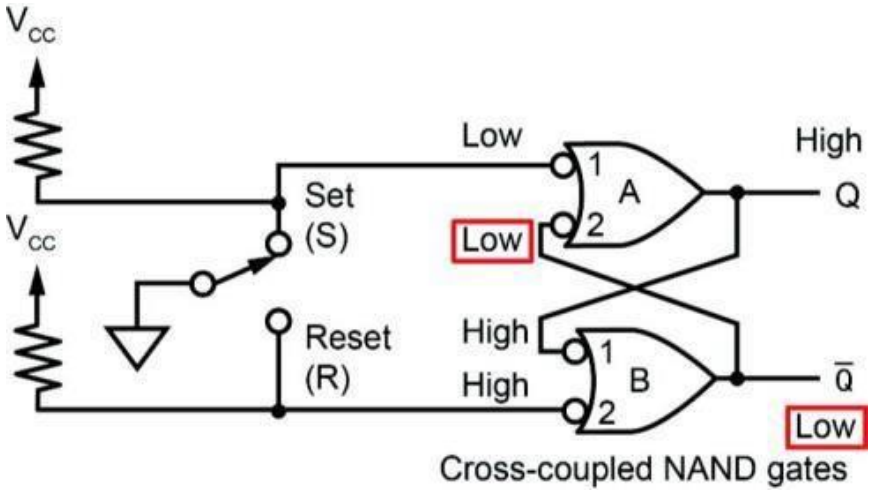
Placing the switch (a two-post connector is used in the circuit block) to SET (S) puts a low at input A1. A low at either input of NAND gate A causes a high at the output (Q).



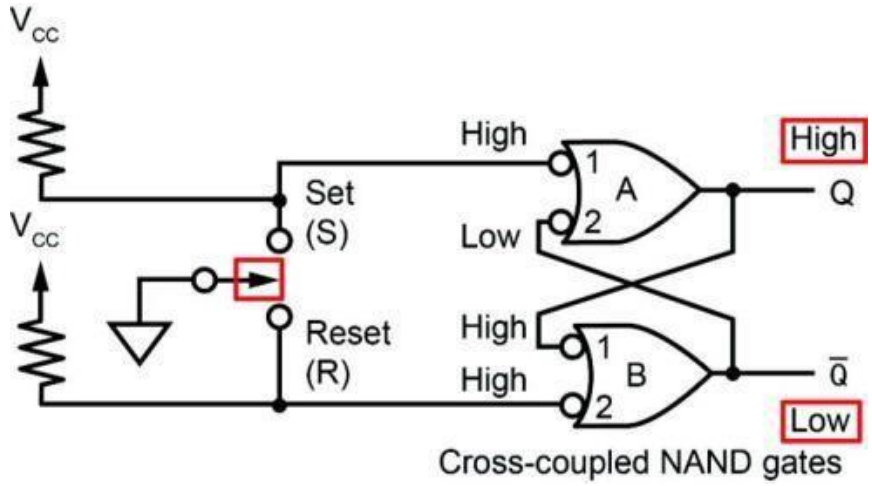
Because Q connects to input B1 of NAND gate B, the two high inputs to gate B cause a low at Q!.



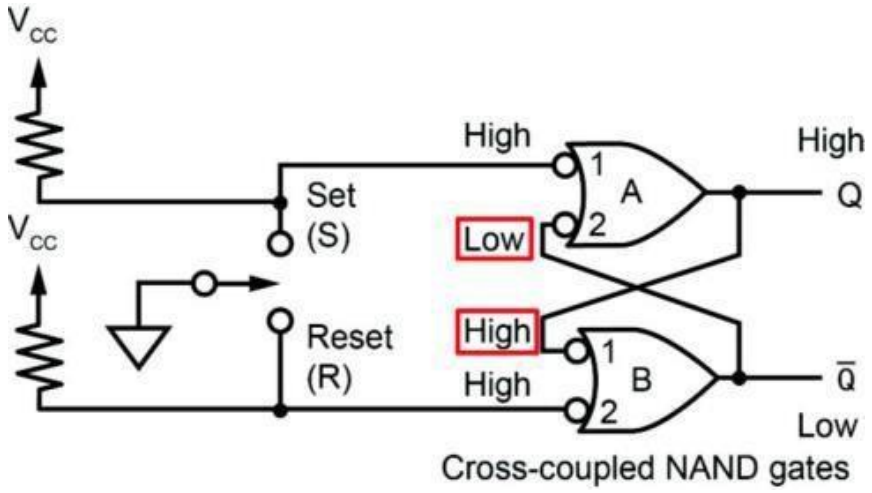
Because Q! connects to input A2 of NAND gate A, input A2 is low.



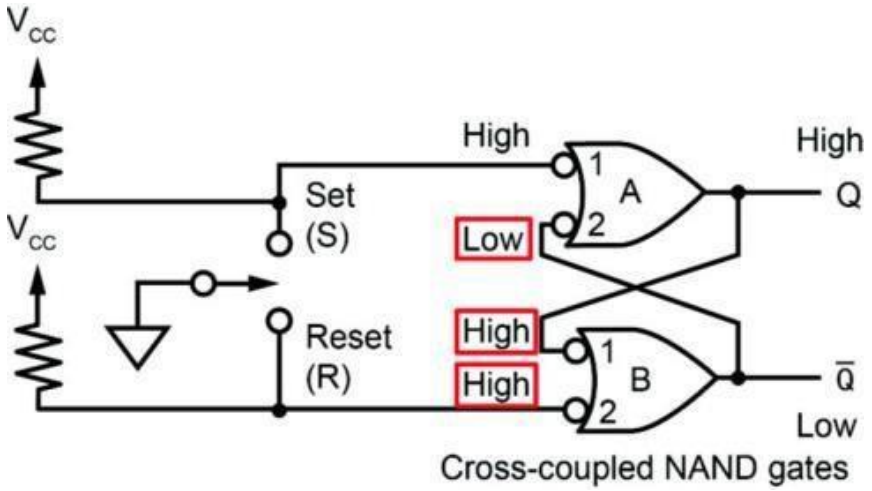
When the switch is open, the Q output remains high and the Q! output remains low because the gates are cross-coupled (this is a property of the cross-coupled gates).



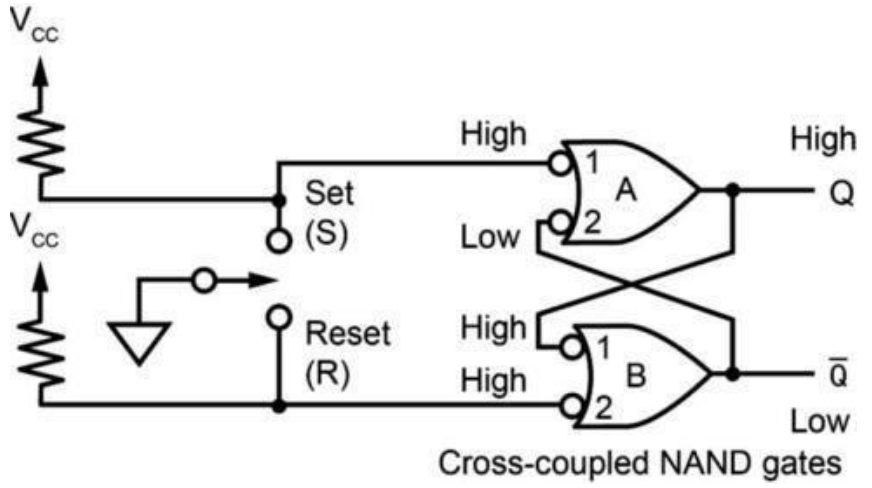
The feedback from gate B (Q!) maintains input A2 low, and the feedback from gate A (Q) maintains input B1 high.



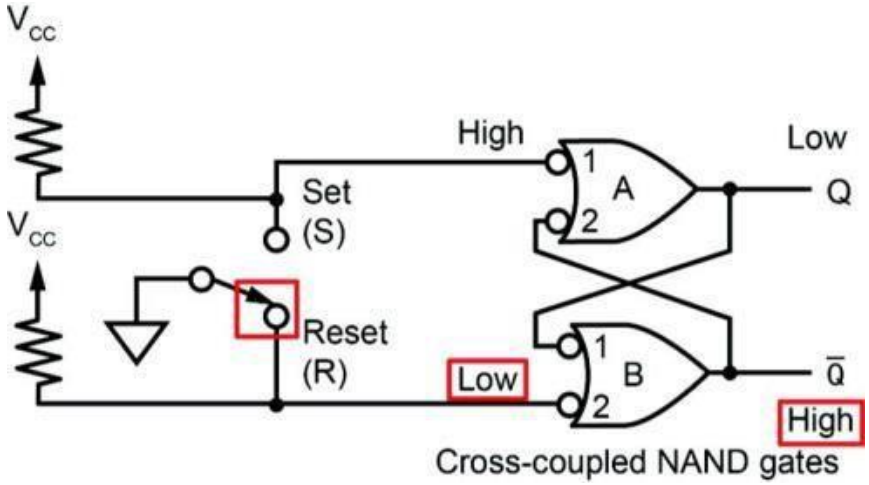
NAND gate A has a low input that is required for a high output (Q), and NAND gate B has two high inputs that are required for a low output (Q!).



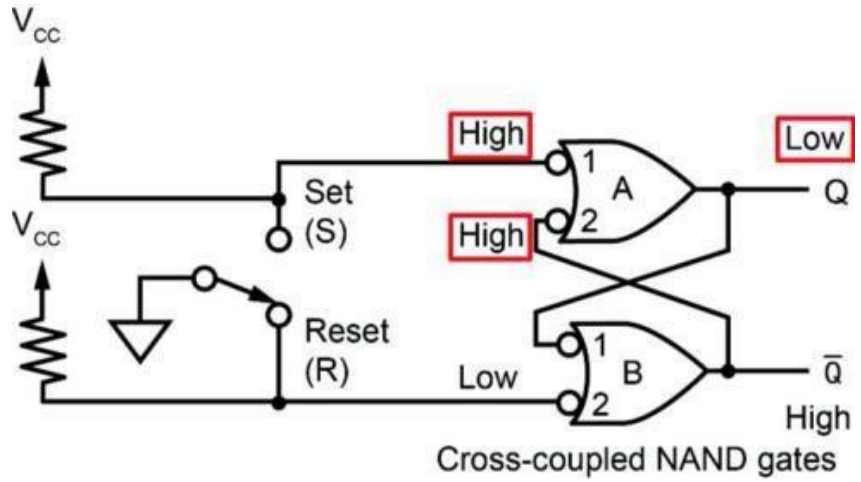
Q: Why does the Q output remain high when the switch is opened?
a. Because the low Q! from gate B connects to input A2 b. Because of the high at input B2
c. None of the above



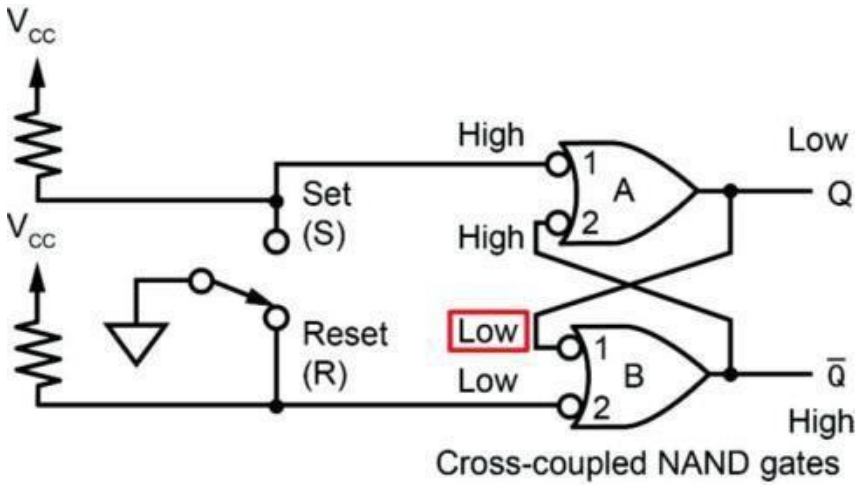
Placing the switch to RESET (R) puts a low at input B2. A low at either input of NAND gate B causes a high output (Q!).



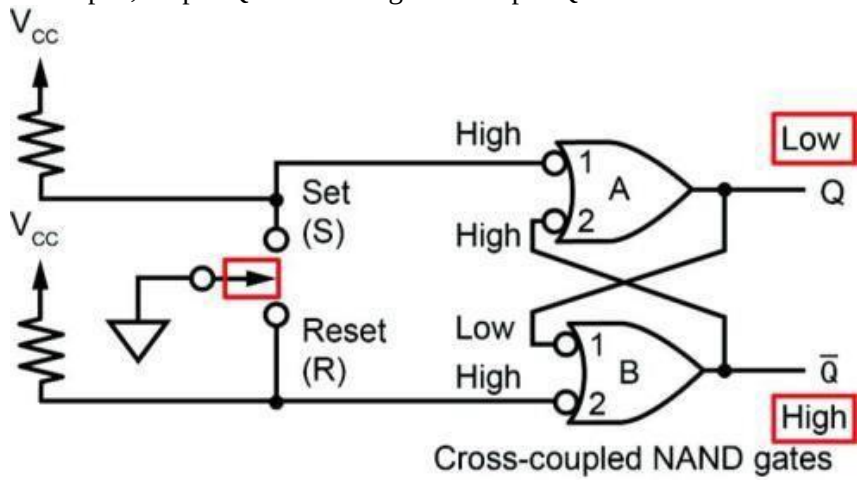
Because Q! connects to input A2 of NAND gate A, the two high inputs at gate A cause a low output (Q).



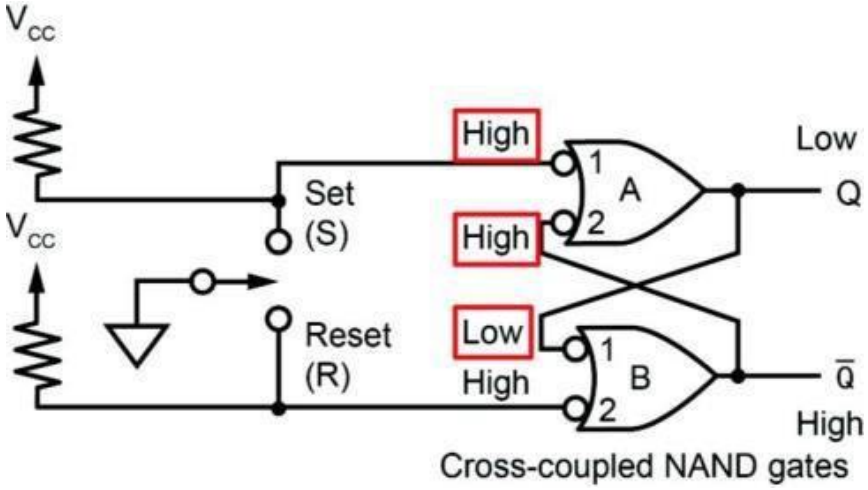
Because Q connects to input B1 of NAND gate B, input B1 is low.



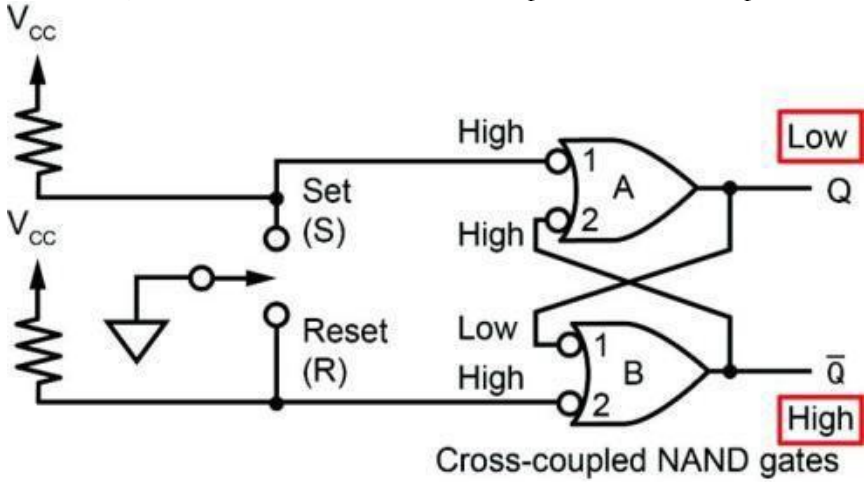
When the switch is open, output Q! remains high and output Q remains low because of the feedback.



NAND gate B has a low input that is required for a high output (Q!), and NAND gate A has two high inputs that are required for a low output (Q).

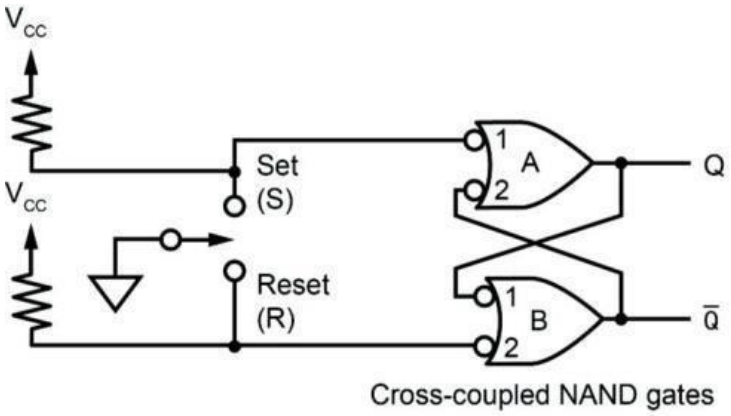


Q! remains HIGH and Q remains LOW until the switch is placed in the SET position, as shown:



When the position of a switch changes, it bounces (makes and breaks contact) a few times before making permanent contact.

Because the Q and Q! debounce a switch contact.
Initially, the switch is in the open position, as follows:

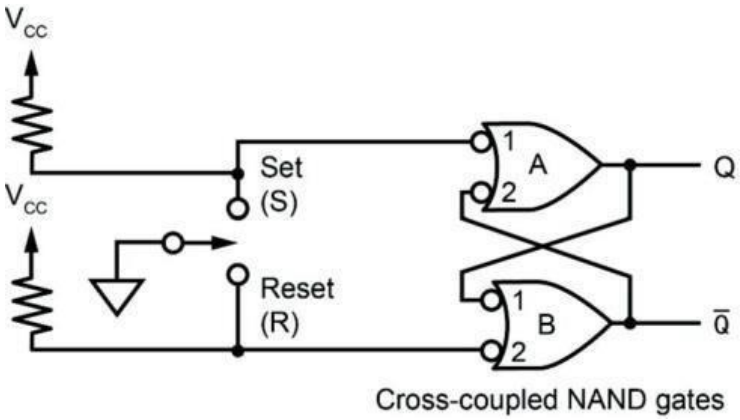


Cross-coupled NAND gates

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	1	1	0
1	1	1	0
1	0	0	1
1	1	0	1
0	0	1*	1*
1	1	Indeterminate	

* Prohibited

Placing the switch in the open position after SET or RESET does not change the output state.

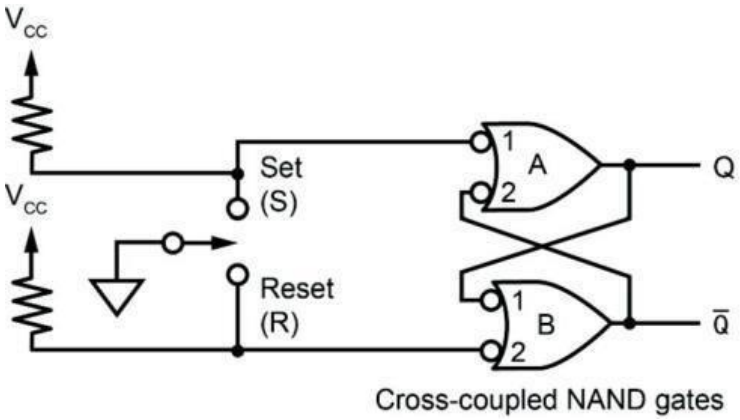


Cross-coupled NAND gates

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	1	1	0
1	1	1	0
1	0	0	1
1	1	0	1
0	0	1*	1*
1	1	Indeterminate	

* Prohibited

However, if a low were put at both the SET and RESET inputs, Q and Q! would be high. This state is prohibited because complementary outputs are desired.

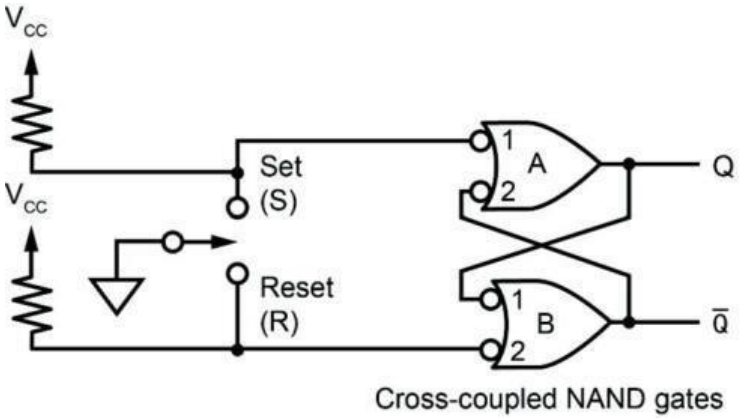


Cross-coupled NAND gates

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	1	1	0
1	1	1	0
1	0	0	1
1	1	0	1
0	0	1*	1*
1	1	Indeterminate	

* Prohibited

Putting a high to the SET and RESET inputs following the prohibited output state (two highs) causes a race condition between the Q and Q! outputs to an indeterminate complementary output condition.



Cross-coupled NAND gates

Inputs		Outputs	
S	R	Q	Q̄
0	1	1	0
1	1	1	0
1	0	0	1
1	1	0	1
0	0	1*	1*
1	1	Indeterminate	

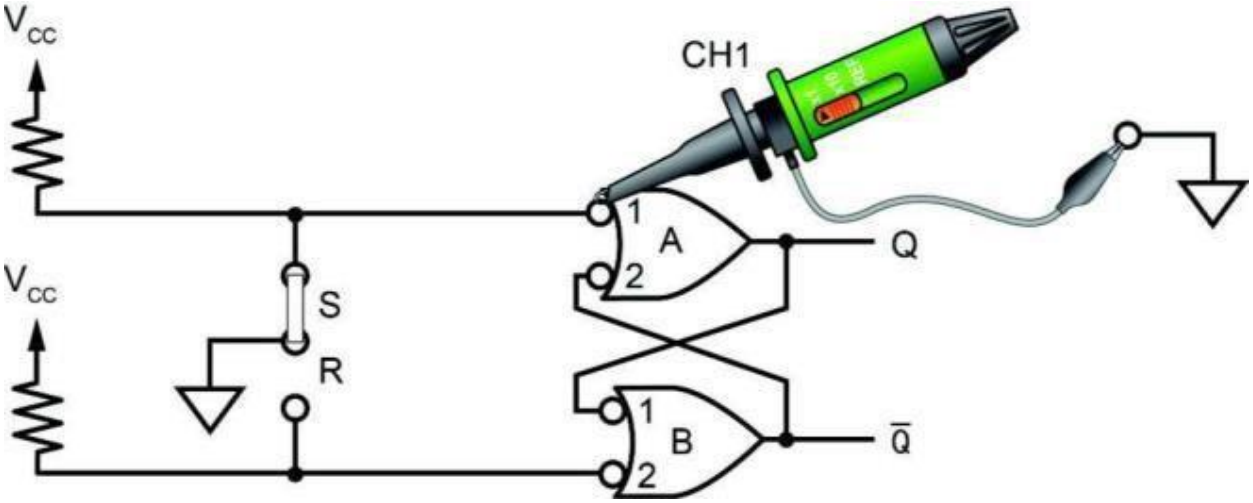
* Prohibited

Hence, complementary outputs (Q and Q!) are desired.

- **PROCEDURE**

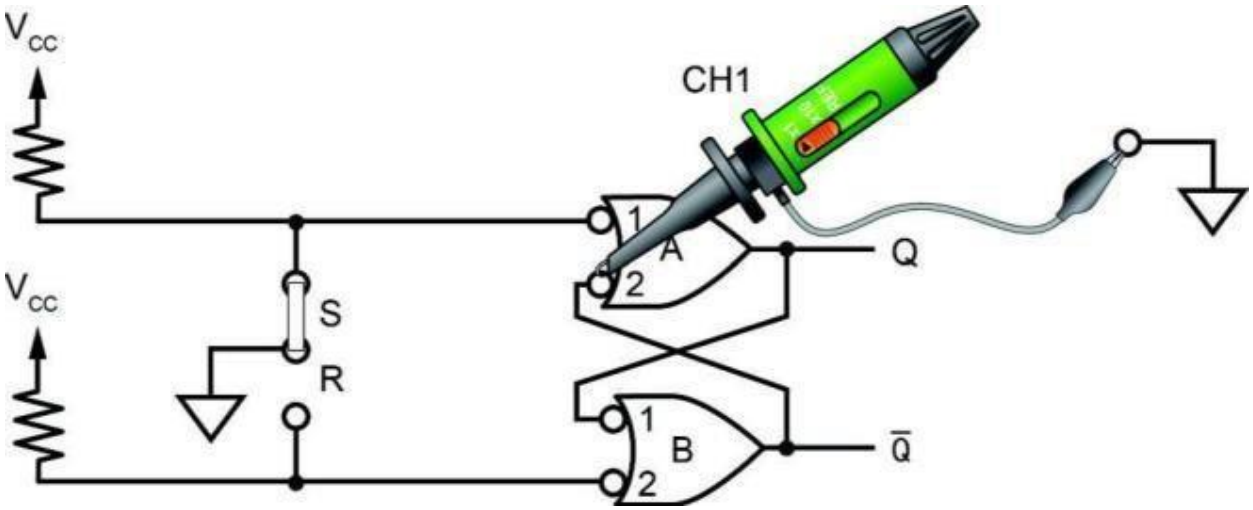
Locate the SET/RESET FLIP-FLOP circuit block.
Place a two-post connector in the S (SET) position to put a logic low (ground) at the S input.
You will be asked to measure the logic levels at the points shown.
Connect the oscilloscope channel 1 probe ground clip to a ground terminal on the circuit board.
Q: The voltage level at input A1 is logic:

a. High b. Low



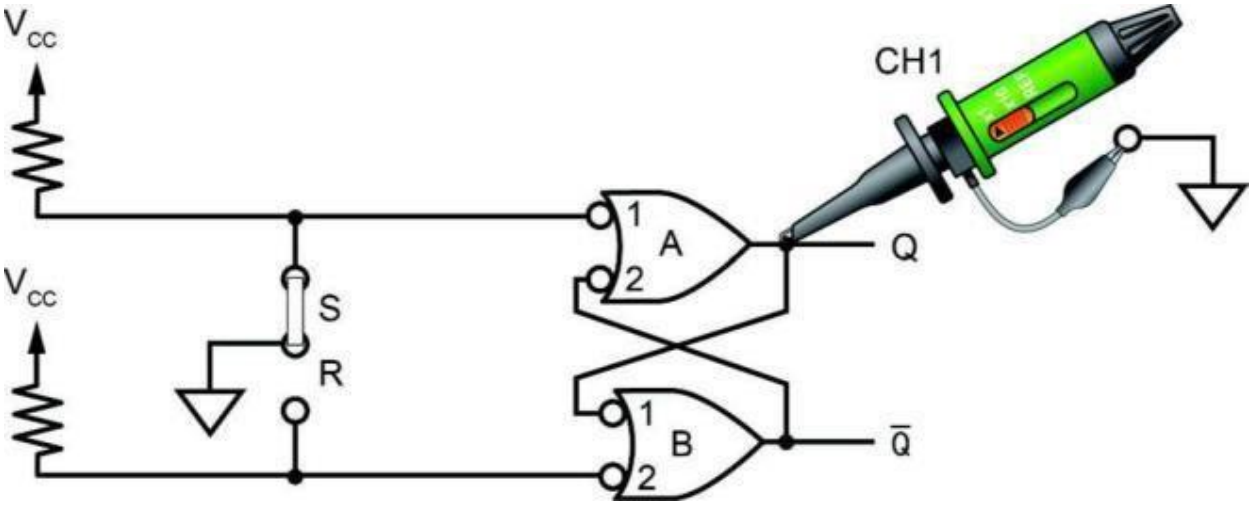
Q: The voltage level at input A2 is logic

a. high. b. low.



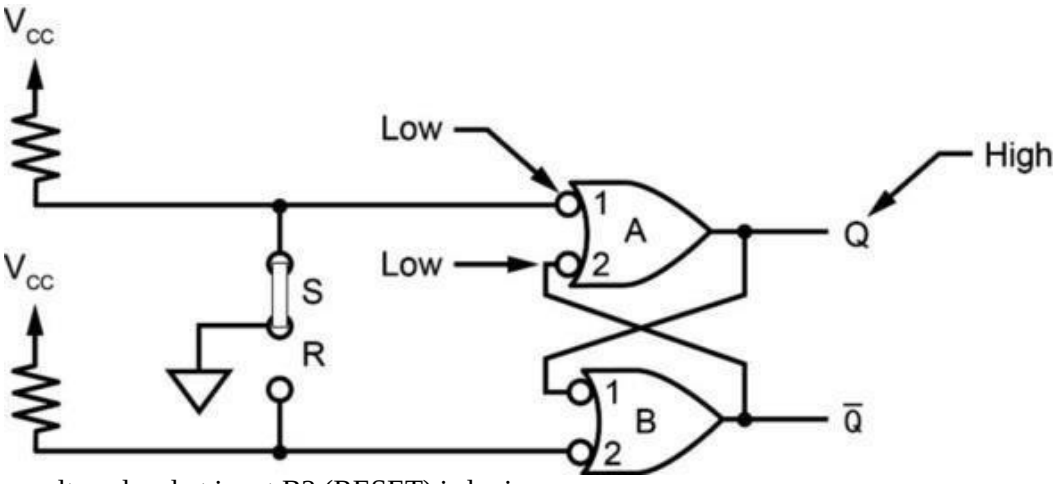
Q: The voltage level at output Q is logic:

a. High b. Low



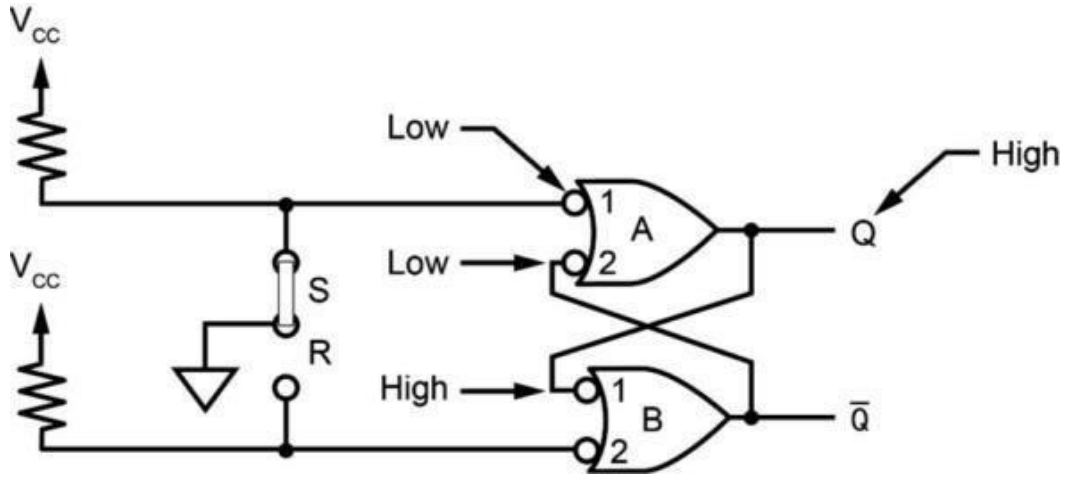
Q: The voltage level at input B1 is logic

a. high. b. low.



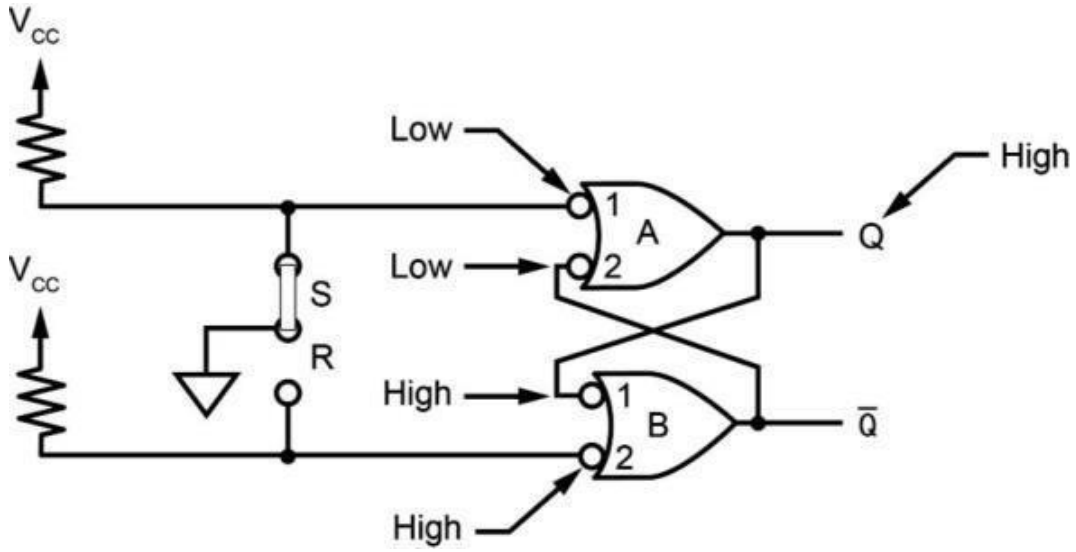
Q: The voltage level at input B2 (RESET) is logic

a. high. b. low.



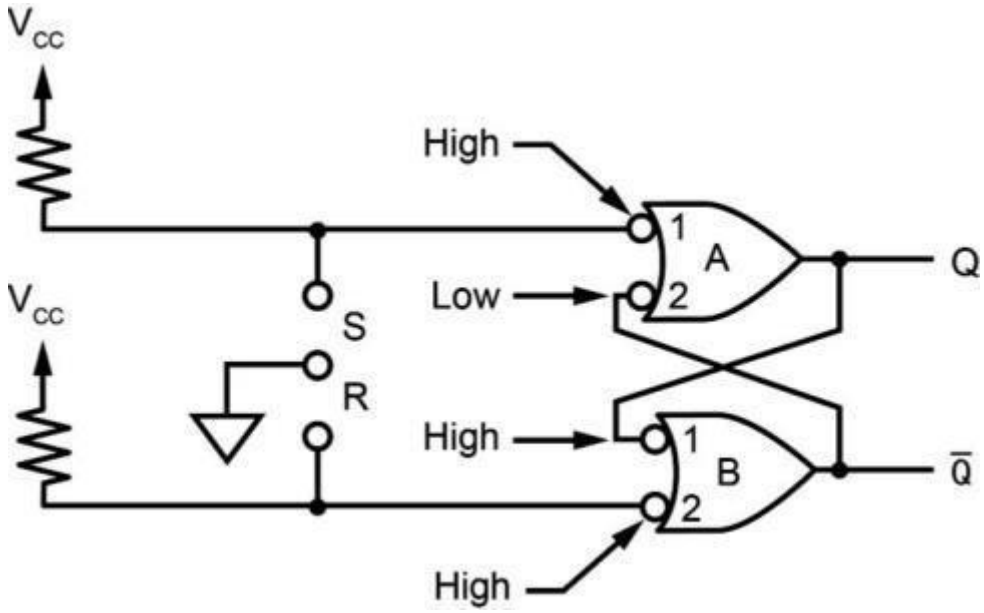
Q: The voltage level at output Q! is

a. high. b. low.



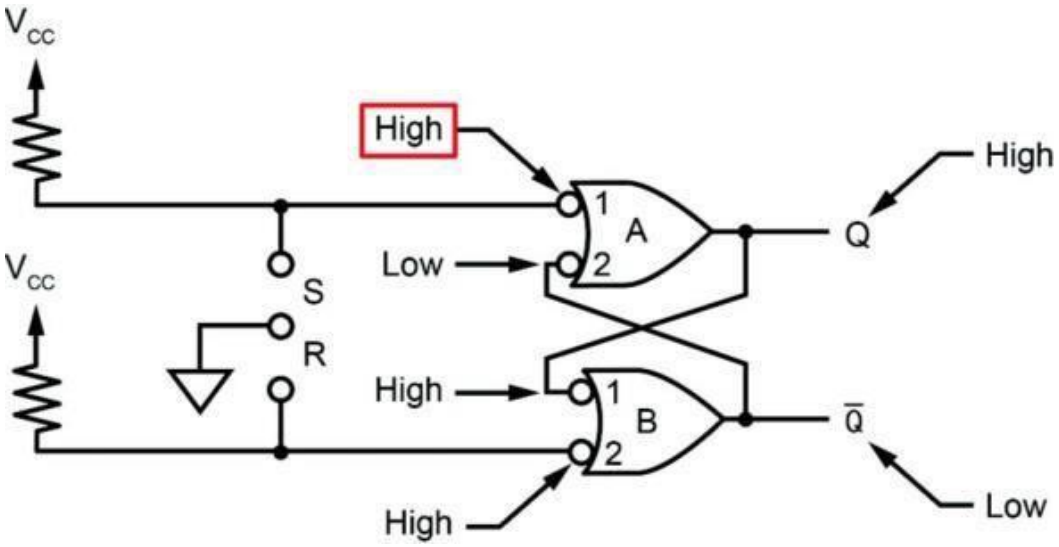
Q: If you changed the S input (A1) from low to high by removing the two-post connector, the output logic levels (Q and Q!):

a. change. b. remain the same.

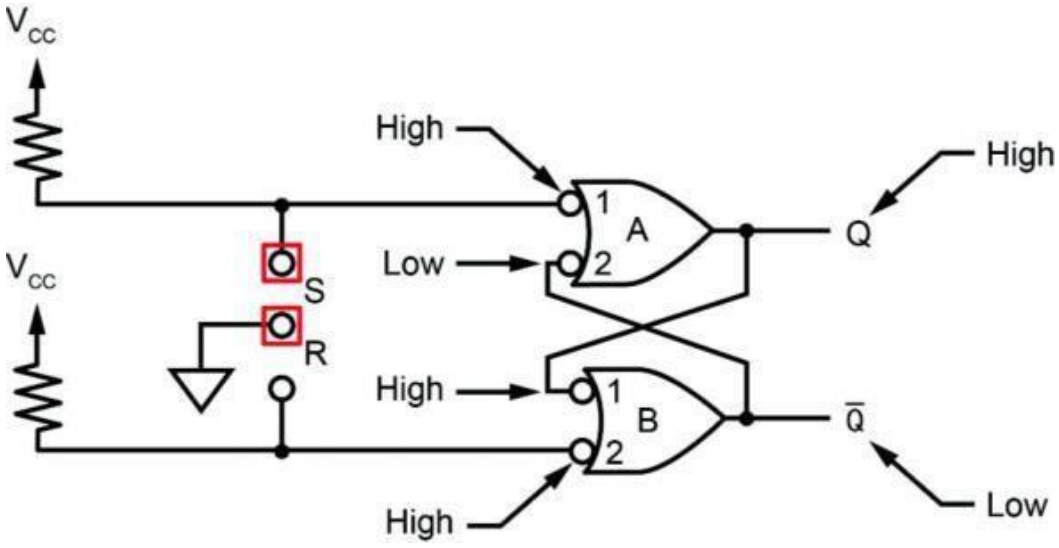


Q: When the S input (A1) changed from low to high, the outputs did not change because of the logic

a. low feedback from gate B (Q!) to gate A.
b. high at input B2 of gate B.
c. Both A and B
d. None of the above

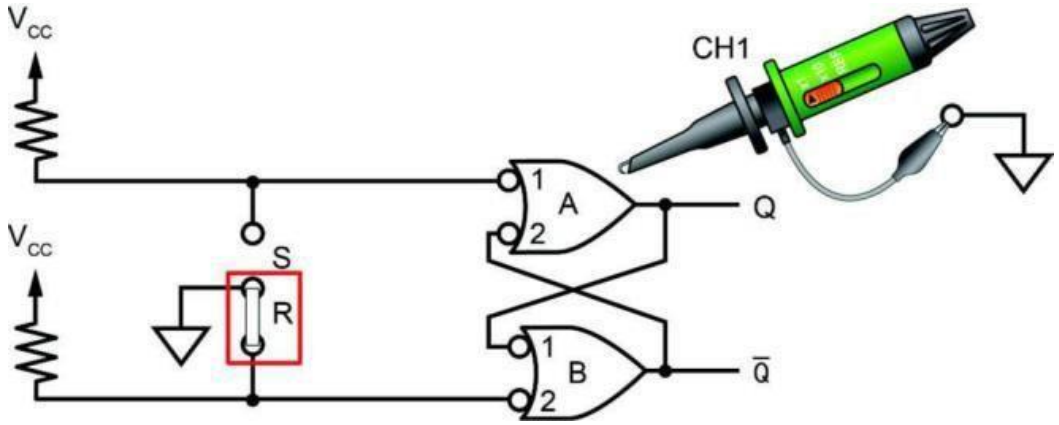


While observing the Q and Q! output signals on the oscilloscope, place the two-post connector in and out of the S position several times to simulate a switch bounce condition.



As the two-post connector was placed in and out of the S position, the logic levels of the outputs
a. did not change. b. changed.

Place the two-post connector in the R (RESET) position. You will be asked to measure the logic levels at the points shown. Connect the channel 1 probe ground clip to a ground terminal on the circuit board.

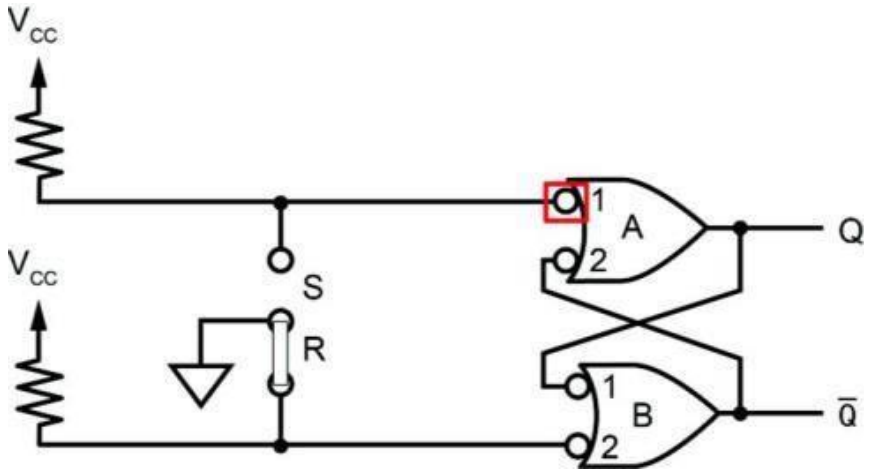


Q: When the two-post connector was connected to the R position:

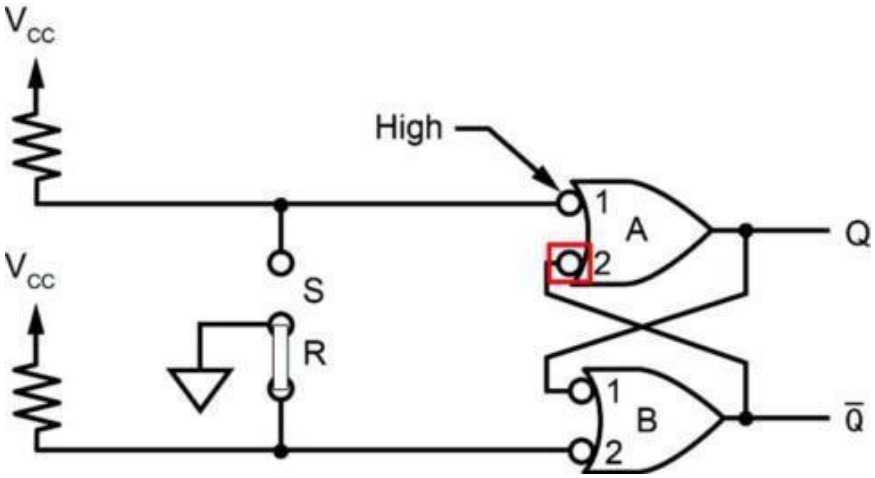
a. The Q output is high and the Q! output is low The Q output is low and the Q! output is high

Q: The voltage level at input A1 is logic:

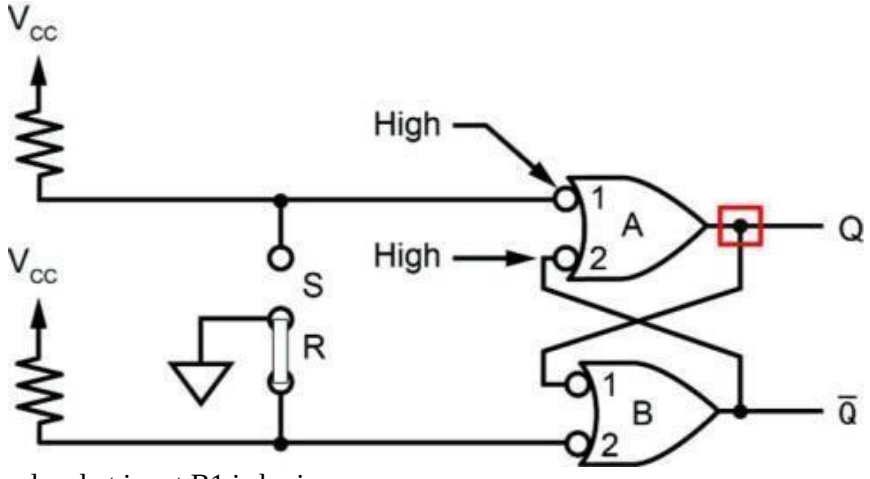
a. High b. Low



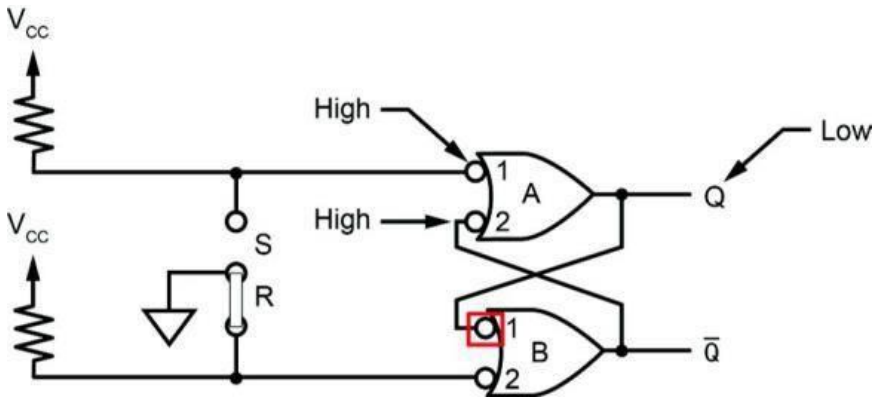
Q: The voltage level at input A2 is logic
a. high. b. low.



Q: The voltage level at Q is logic:
a. high. b. low.

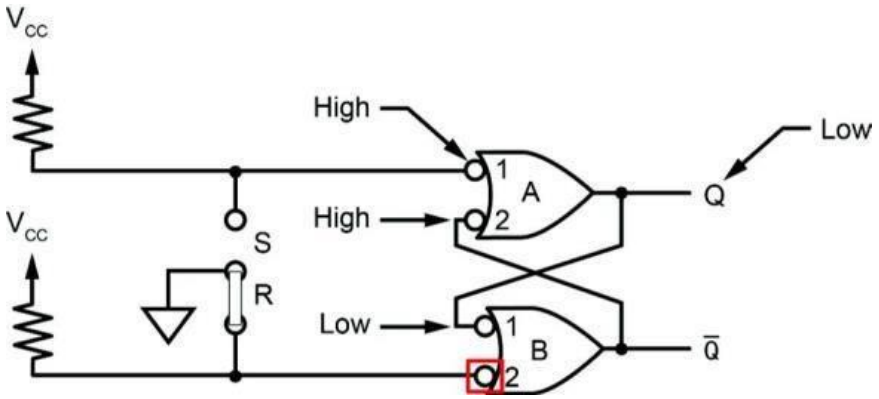


Q: The voltage level at input B1 is logic
a. high. b. low.



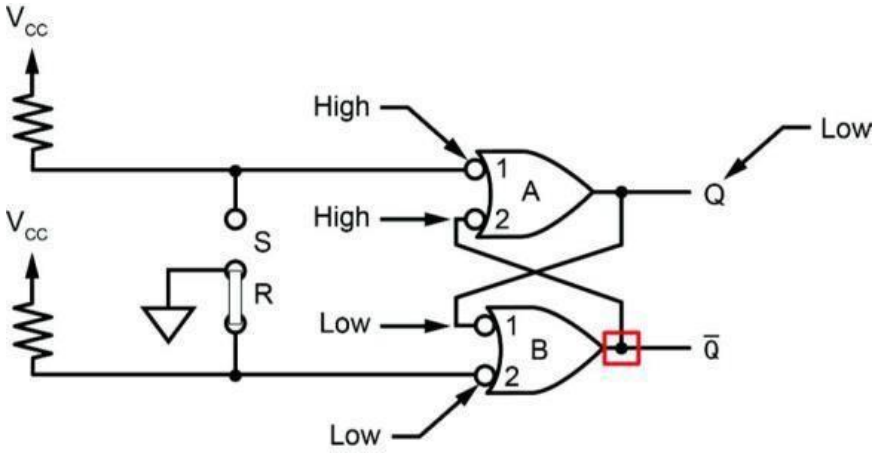
Q: The voltage level at input B2 (RESET) is logic

a. high. b. low.



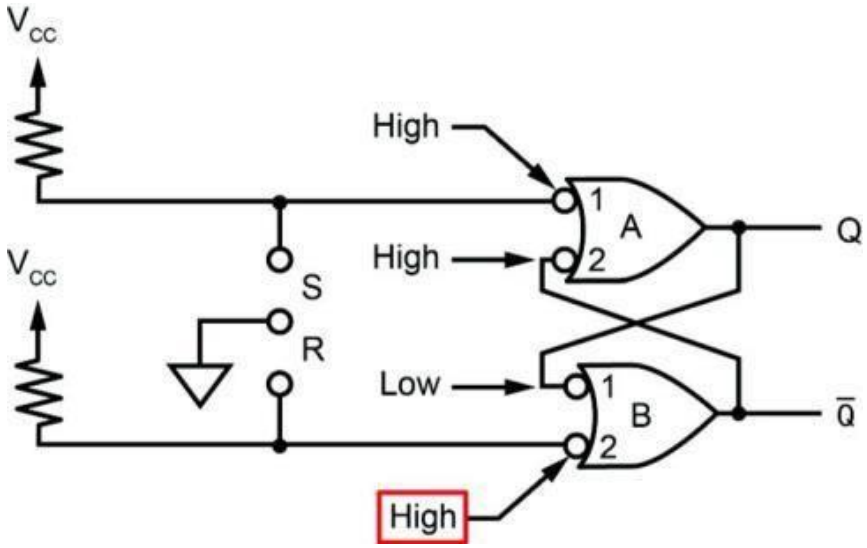
Q: The voltage level at the output Q!

a. high. b. low.



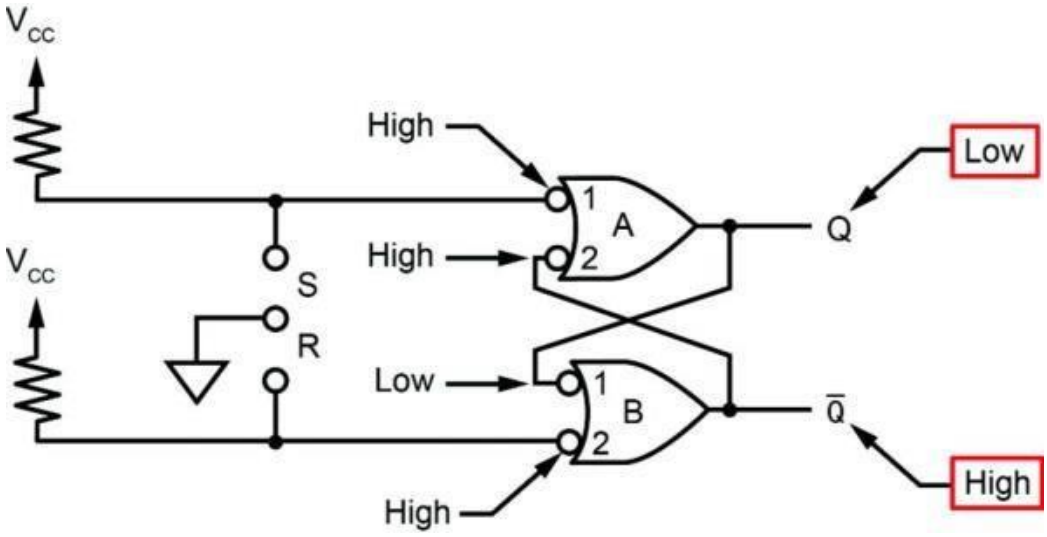
Q: If you changed the R input from low to high by removing the two-post connector from the circuit, the output logic levels (Q and Q!) would

a. change. b. remain the same.

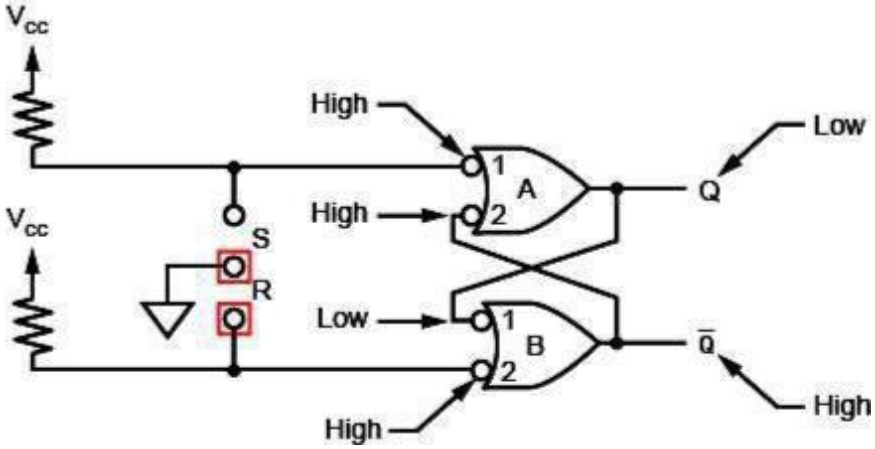


Q: When the R input (point B2) changed from low to high, the outputs did not change because of the logic

a. low feedback from gate A (Q) to gate B. b. high at input A1 of gate B.

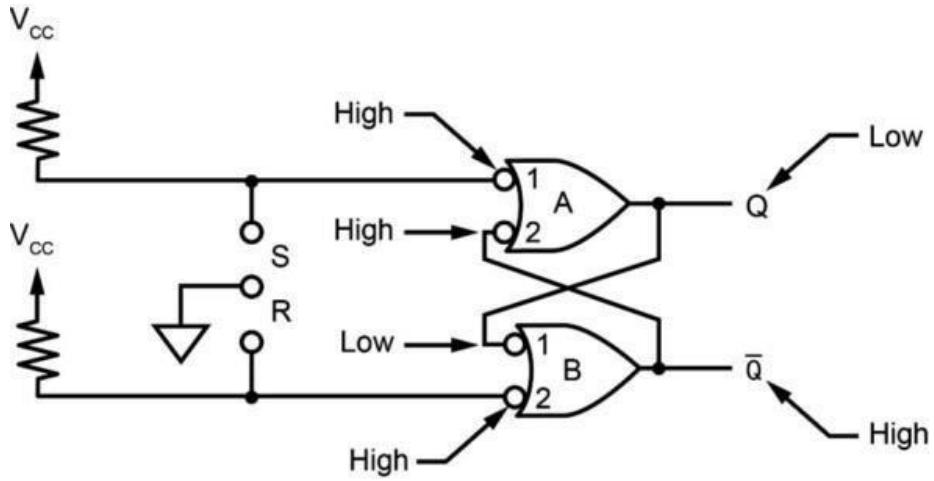


Place the two-post connector in and out of the R position several times to simulate a switch bounce condition.



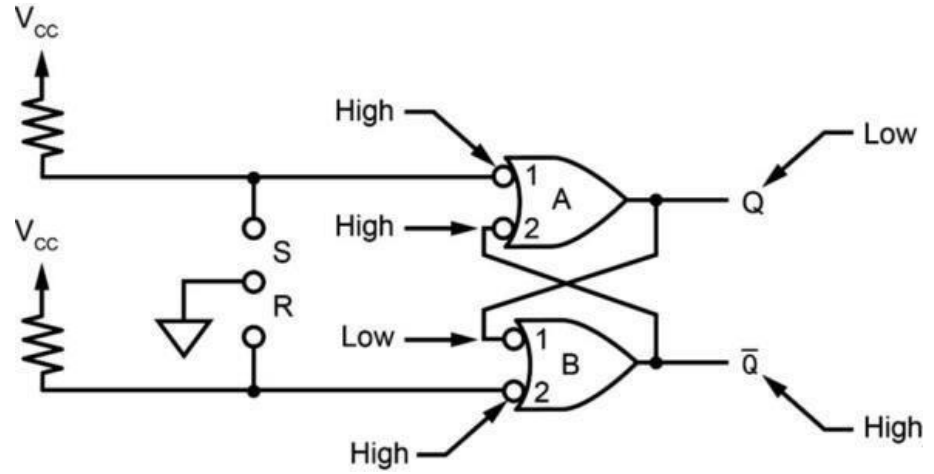
As you place the two-post connector in and out of the R position, the logic levels of the circuit outputs

a. do not change. b. change.

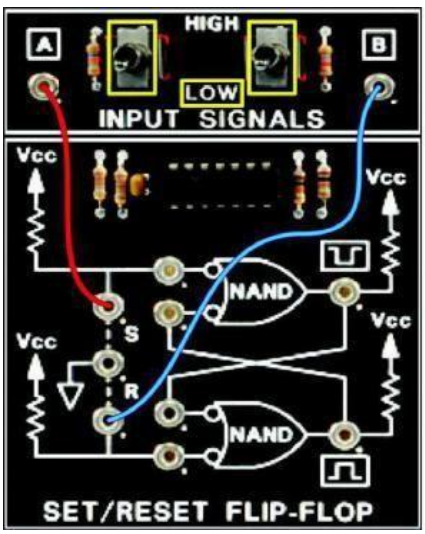


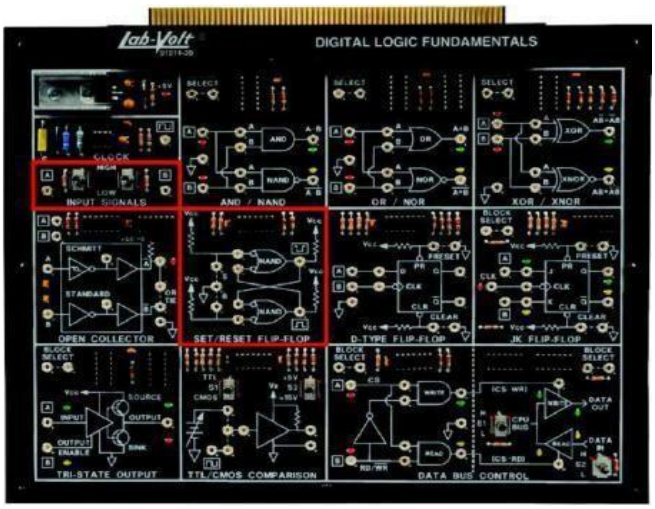
Q: Based on your data, the Q and Q! outputs

a. are complementary. b. can have the same or opposite logic levels.

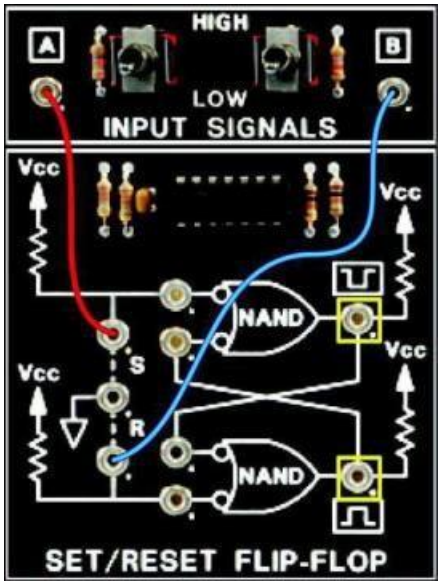


Connect the circuit shown. Place both INPUT SIGNALS toggle switches in the LOW condition with two low inputs.





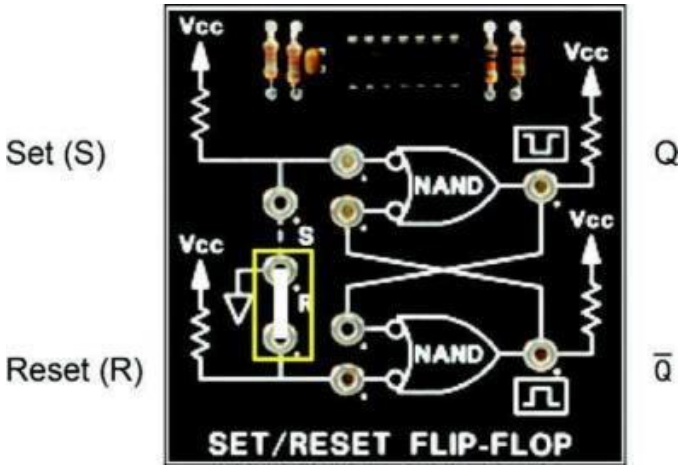
Q: Connect the oscilloscope channel 1 probe to Q and the channel 2 probe to Q!. Q and Q! are both
a. high. b. low.



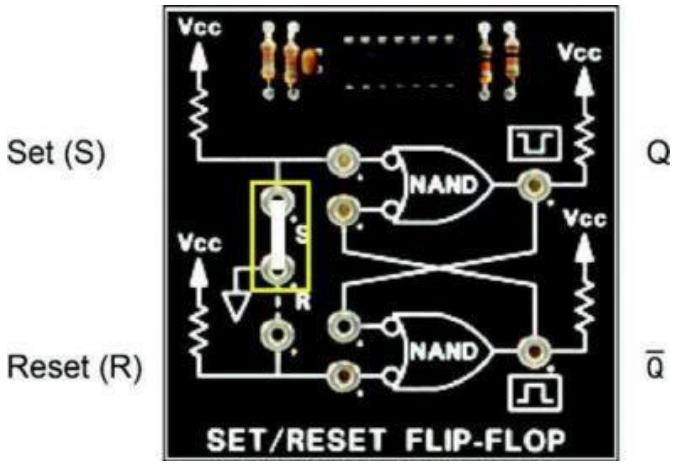
- **CONCLUSION**
  - The SR flip flop consists of two cross-coupled NAND gates.
  - The cross-coupled gates have a feedback property.
  - When either input is logic low at either gate within the flip-flop, the output at that gate is logic high.
  - SR inputs of 0 and 0 result with a prohibited state with similar outputs (Q and Q!).
  - SR inputs of 1 and 1 result with an indeterminate state.
  - It is desirable to only use non-similar input values.

- **REVIEW QUESTIONS**

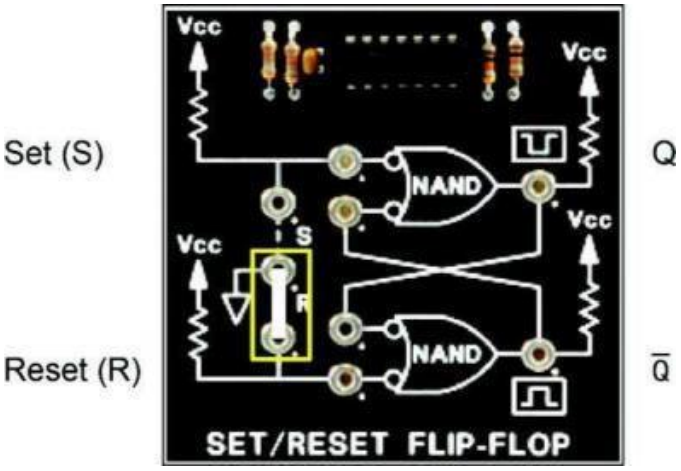
1. Locate the SET/RESET FLIP-FLOP circuit block.
Put a two-post connector in the R position to reset the set/reset. Q should be logic high.



Place CM switch 9 in the ON position.
Move the two-post connector to the S position. Measure the logic levels of the outputs.

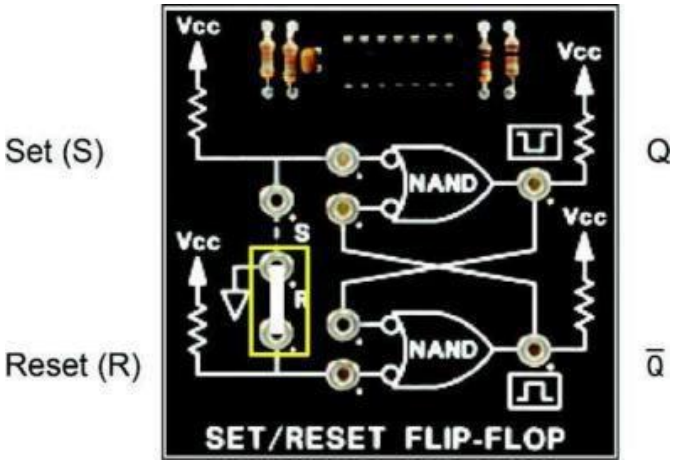


Move the two-post connector back to the R position. Measure the logic levels of the outputs.



Q: The flip-flop:

a. operates correctly.
b. cannot be set.
c. cannot be reset.
d. outputs are not complementary.



Lab 5B: D Flip-Flop

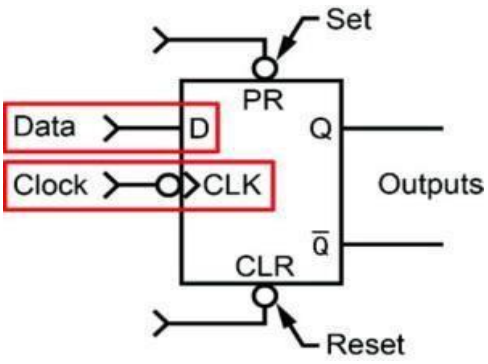
- **OBJECTIVE**

When you have completed this exercise, you will be able to determine the characteristics of a D-type flip-flop and confirm the results with an oscilloscope.

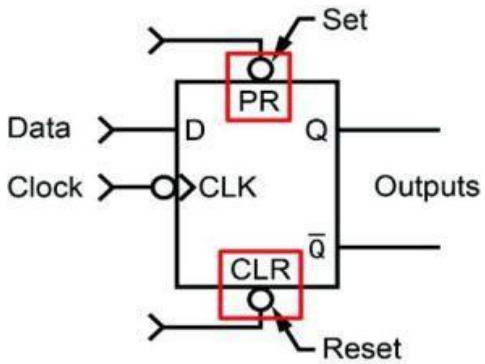
- **REQUIREMENTS**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - PC or Laptop computer.
  - An oscilloscope

- **EXERCISE DISCUSSION**

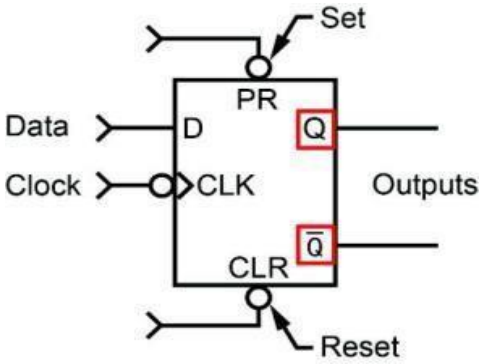
The D-type flip-flop has one data input (D) and a clock input (CLK).



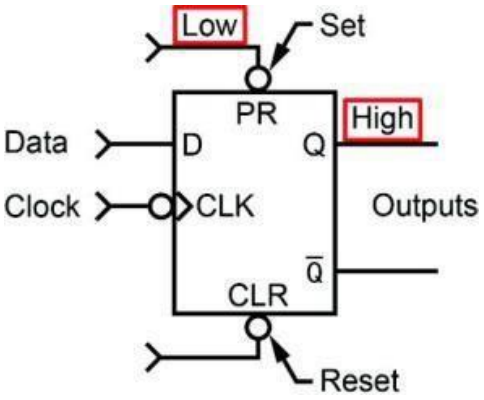
There are two asynchronous inputs: Set (PR) and Reset (CLR).



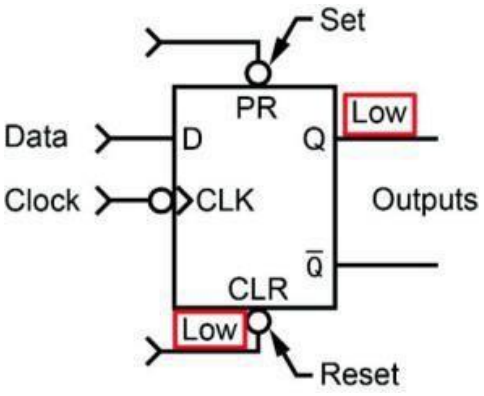
The two outputs, Q and Q!, are complementary.



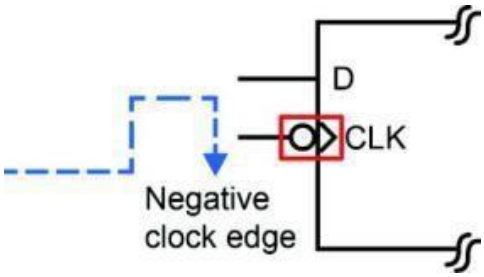
A low (logic 0) at PR sets Q high (logic 1).



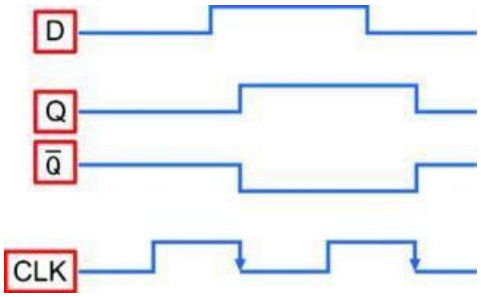
A low at CLR resets Q low.



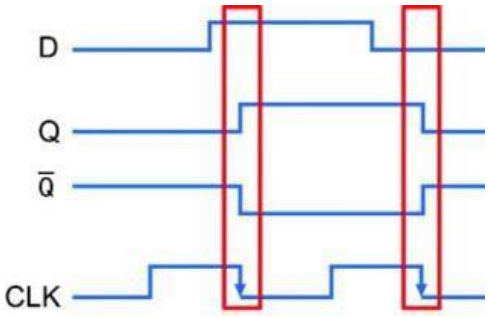
When either PR or CLR are logic low, the data and clock signals have no effect on Q and Q!. The small circle and triangle at the CLK input indicate that the negative edge of the clock signal activates the data (D) input.



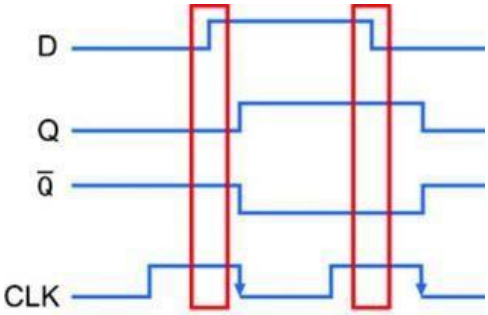
The timing diagram shows the relationship between the data input (D), the outputs (Q and Q!), and the clock signal (CLK).



Q equals the D input after the negative edge of the CLK. Q! is the complement of D and Q.

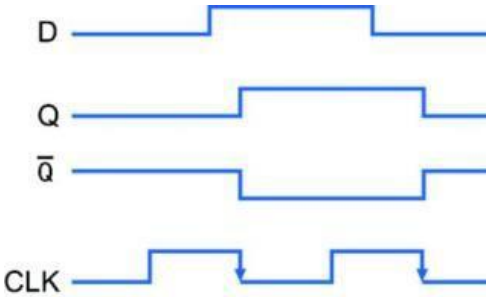


The current value at Q is held until there is another negative edge of the CLK signal.



Q: The Q output is logic 1. If input D is logic 0 during the next negative edge of the clock signal, the Q output

a. stays logic 1. b. changes to logic 0.



The following table shows the behavior of the D flip-flop. The logic states of D and CLK do not affect the outputs when either the PR or CLR is LOW.

Inputs				Outputs	
Preset (PR)	Clear (CLR)	Clock (CLK)	Data (D)	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
1	1	1	X	Q	$\overline{Q}$
1	1	↓	1	1	0
1	1	↓	0	0	1
1	1	0	X	Q	$\overline{Q}$

X = Does not affect output

↓ = Negative clock transition (high-to-low) required

Q & $\overline{Q}$ = The level established from the last negative clock transition is maintained.

Q: If PR is logic 0, CLR is logic 1, and D is logic 0, what logic state will Q be after the next negative edge of the CLK?

a. logic 0 b. logic 1

Q: If PR is logic 1, CLR is logic 1, and D is logic 0, what logic state will Q be after the next negative edge of the CLK?

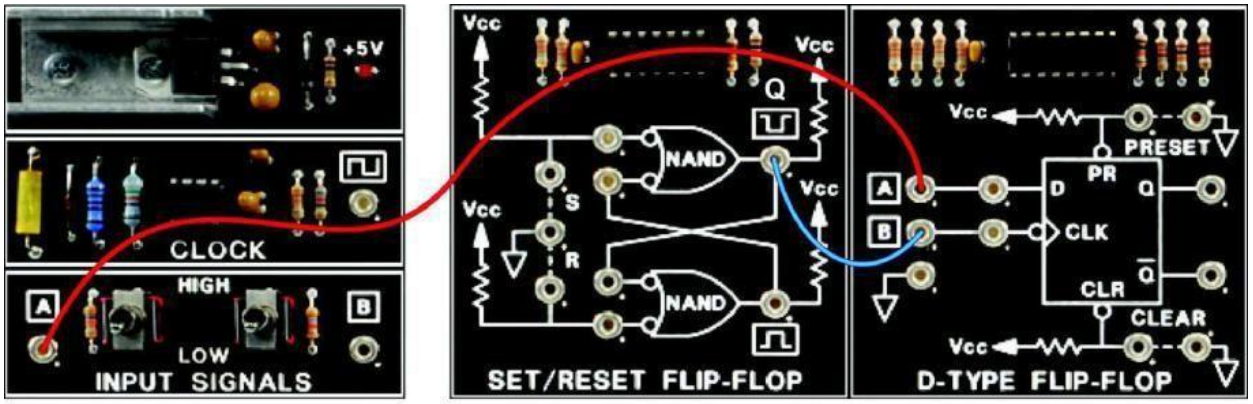
a. logic 0 b. logic 1

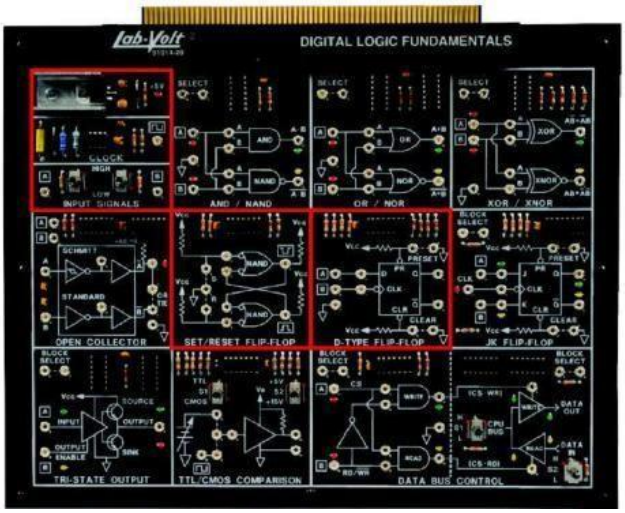
Q: If PR is logic 1, CLR is logic 1, and D is logic 1, what logic state will Q be when the CLK changes from logic 0 to logic 1?

a. Q will remain in its existing state. b. logic 1

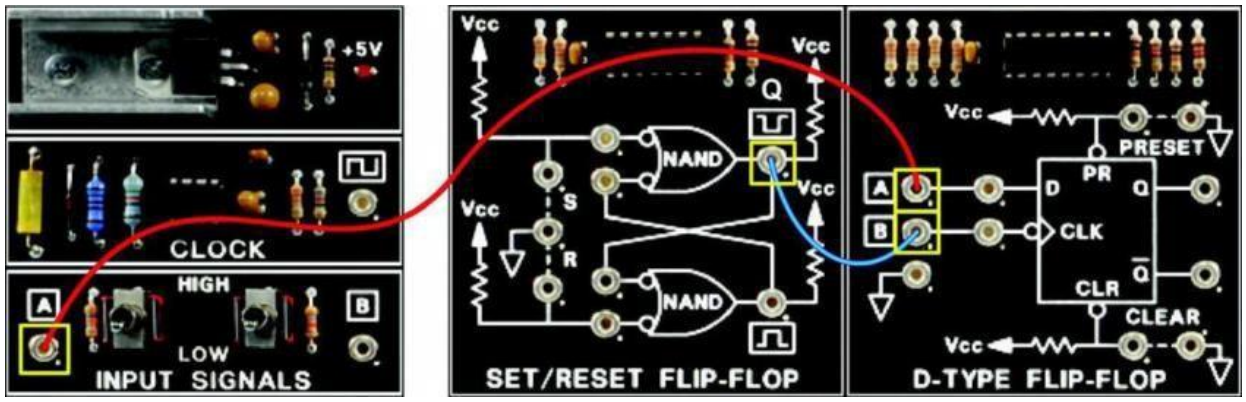
- **PROCEDURE**

Locate the INPUT SIGNALS, SET/RESET FLIP-FLOP, and D-TYPE FLIP-FLOP circuit blocks.

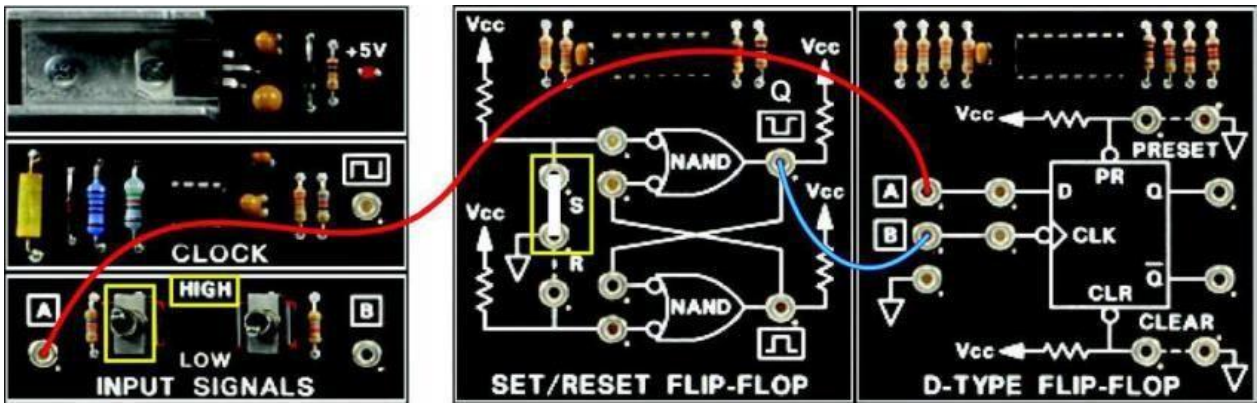




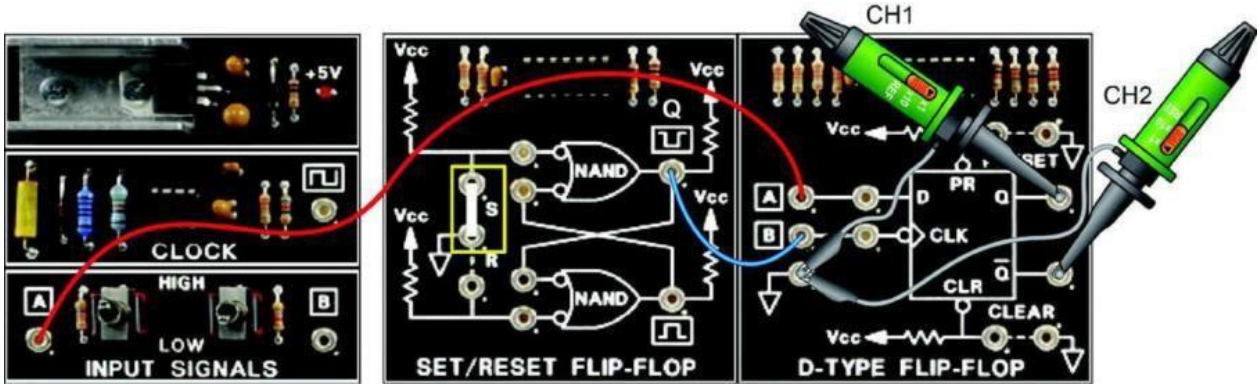
Connect A at the INPUT SIGNALS circuit block to A (D input) on the D-TYPE FLIP-FLOP circuit block. Connect the Q output of the SET/RESET FLIP-FLOP circuit block to B (CLK input) on the D-TYPE FLIP-FLOP circuit block.



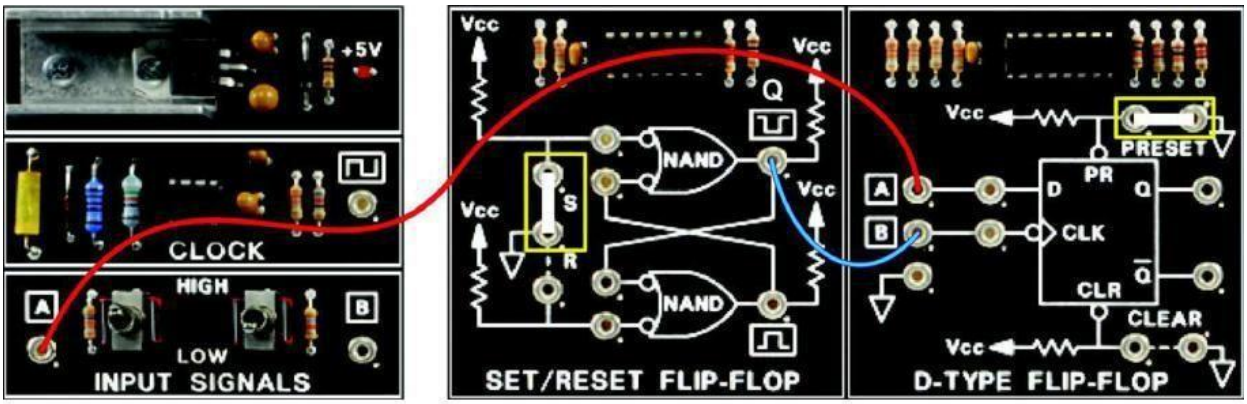
Set toggle switch A in the HIGH position to put a logic high (1) at the D input. Place a two-post connector in the S (SET) position on the SET/RESET FLIP-FLOP circuit block. This puts a high (1) clock signal to CLK.

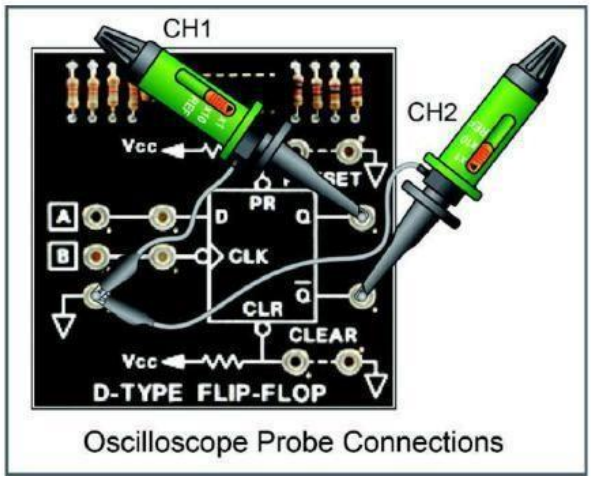


Connect the oscilloscope channel 1 probe to the Q output, and connect the channel 2 probe to the Q! output. Connect the probe ground clips to a ground terminal on the circuit board.



Place a two-post connector at the Preset switch.





Observe the logic states of Q (channel 1) and Q! (channel 2) on the oscilloscope screen to answer the following questions.

Preset Output Logic States

Q: The Q output is

a. logic 1. b. logic 0.

Q: The Q! output is

a. logic 1. b. logic 0.

Q: Are the Q and Q! outputs complementary?

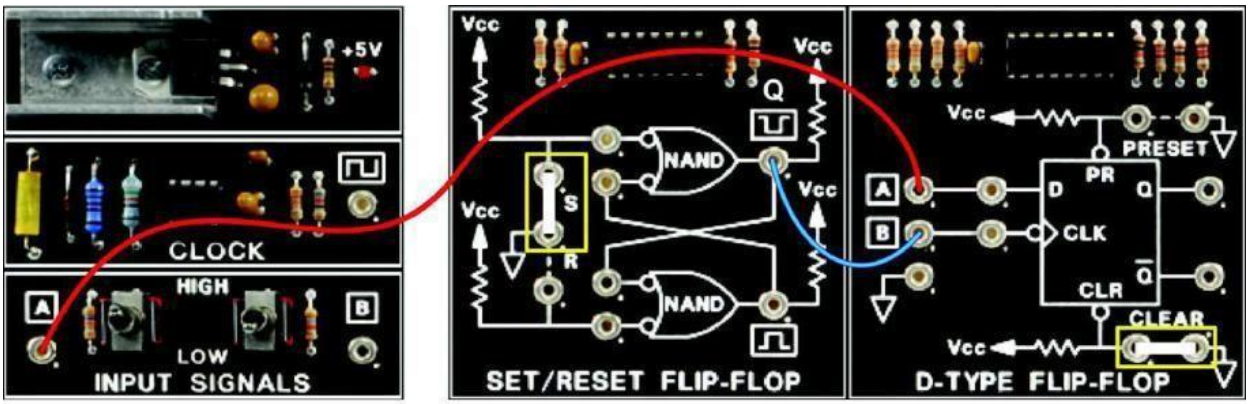
a. yes b. no

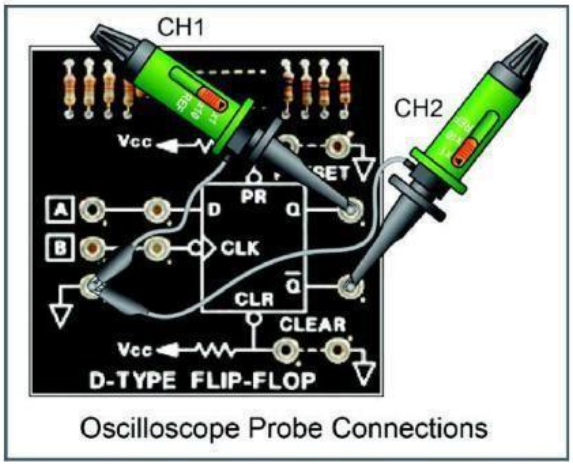
Remove the two-post connector at PRESET.

Q: Did the Q and Q! outputs remain logic 1 and logic 0, respectively?

a. yes b. no

Place the two-post connector at the CLEAR switch in the D flip-flop. This puts a logic 0 (low) at CLEAR.





Clear Output Logic States

Q: The Q output is

a. logic 1. b. logic 0.

Q: The Q! output is

a. logic 1. b. logic 0.

Q: Are the Q and Q! outputs complementary?

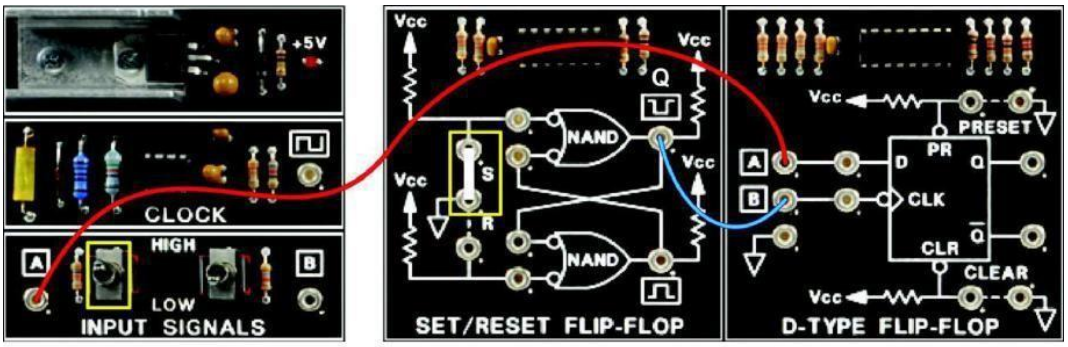
a. yes b. no

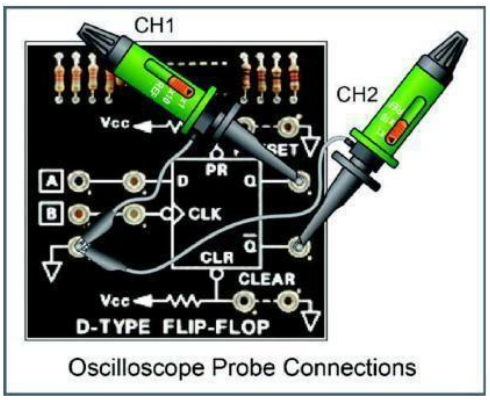
Remove the two-post connector at CLEAR.

Q: Did the Q and Q! outputs remain logic 0 and logic 1, respectively?

a. yes b. no

Toggle switch A from HIGH to LOW and back to HIGH on the INPUT SIGNALS circuit block.





Oscilloscope Probe Connections

Q: Did the Q and Q! output states change when the data input logic state was changed?

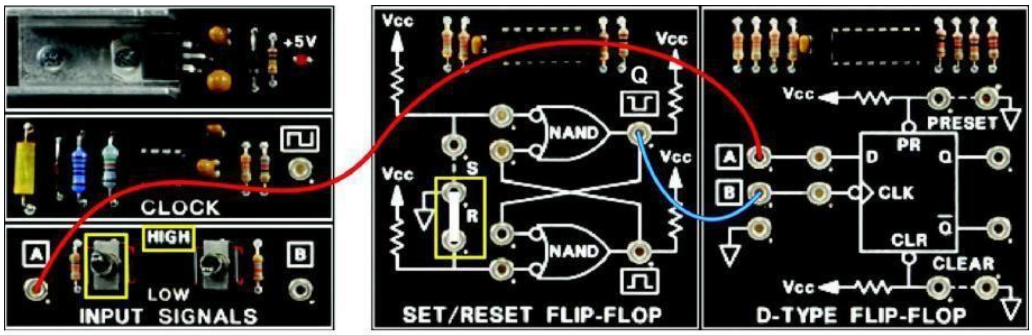
a. yes b. no

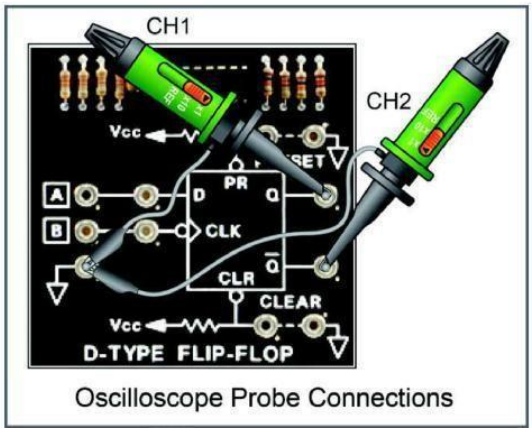
Q: Q and Q! did not change because the Q and Q! outputs respond to the data signal

a. when the clock signal is logic 0. b. only on the negative edge (from high to low) of the clock signal.

The data signal should be logic 1 (toggle switch A set to HIGH).

Q: While observing the Q and Q! outputs on the oscilloscope screen, change the clock signal from logic 1 to 0 by setting the two-post connector from S to R on the SET/RESET FLIP-FLOP circuit block.





Q: The Q output

a. changed to logic 1. b. stayed at logic 0.

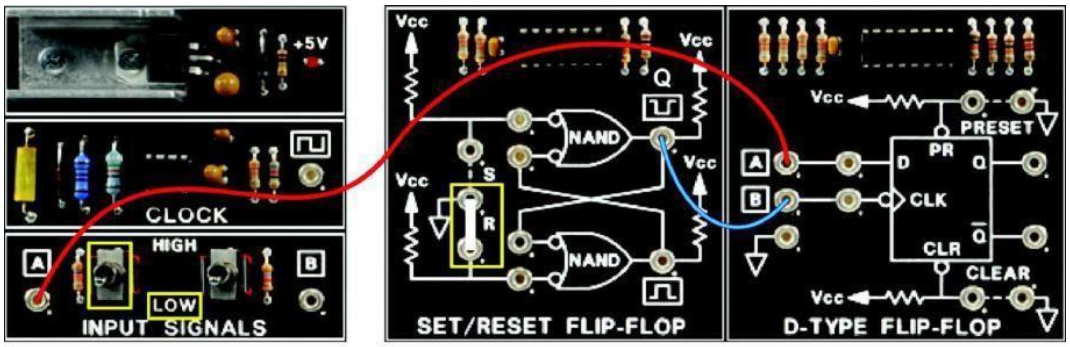
Q: The Q! output is

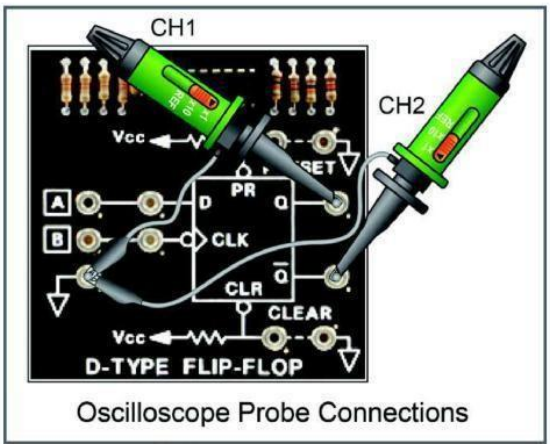
a. logic 1. b. logic 0.

Q: Why did Q go to logic 1 and Q! to logic 0?

a. Because the data input (D) was logic 1 during the negative edge of the clock signal
b. Because the Q and Q! outputs change on a negative clock signal

While observing the Q and Q! outputs on the oscilloscope screen, set the data signal to logic 0 by placing toggle switch A to LOW on the INPUT SIGNALS circuit block.

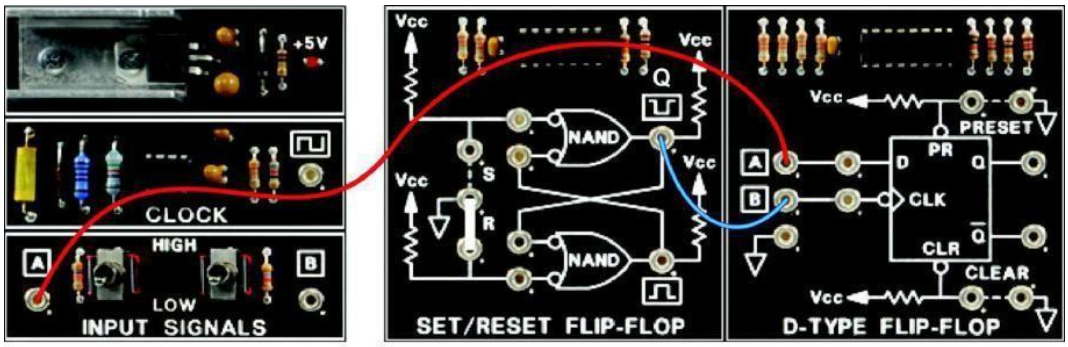


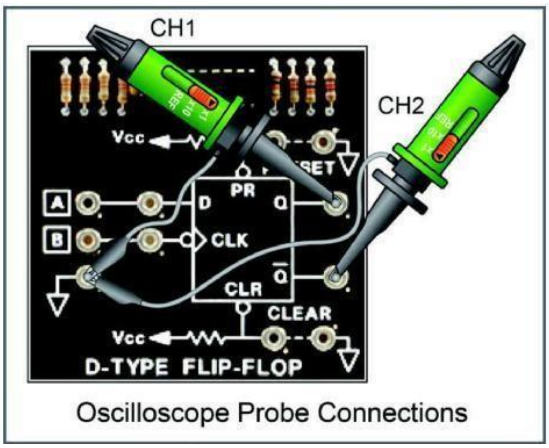


Q: Did the Q and Q! output states change when the data input logic state was changed to logic 0?
a. yes b. no

Q: What will make the Q and Q! output states respond to a data input change from logic 1 to 0?
a. a logic 0 signal at PRESET b. a negative edge of a clock signal

While observing the Q and Q! outputs on the oscilloscope screen, create a negative edge of a clock signal by placing the two-post connector to the S position and then back to the R on the SET/RESET FLIP-FLOP circuit block.





Q: Is there a negative edge of the clock signal?

a. yes b. no

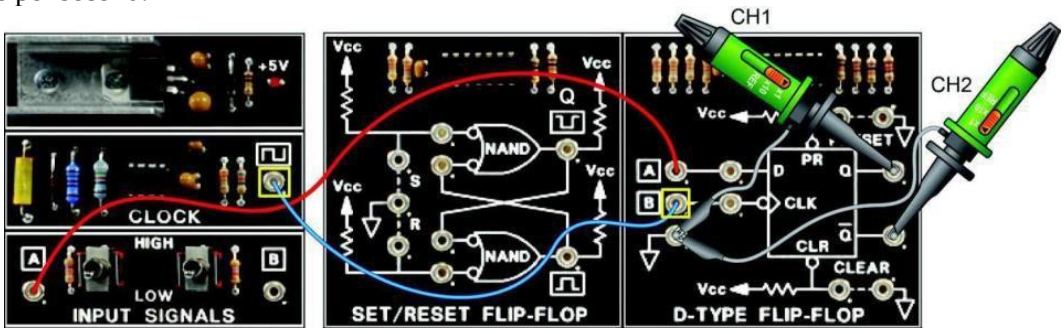
Q: The Q output is

a. logic 1. b. logic 0.

Q; he Q! output is

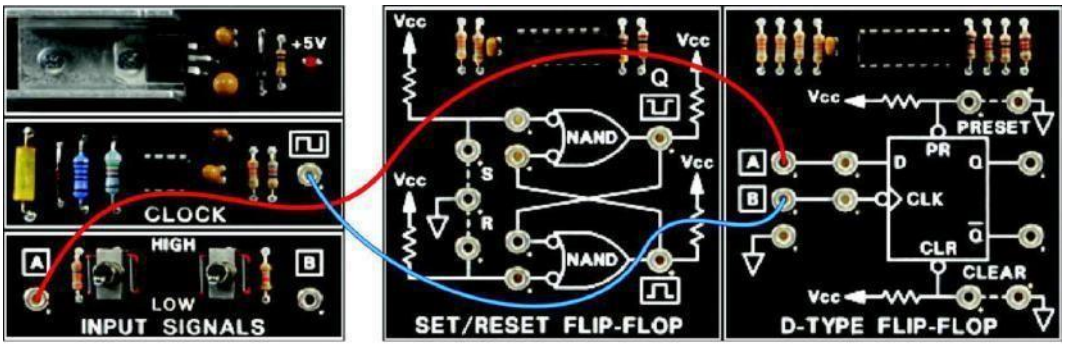
a. logic 1. b. logic 0.

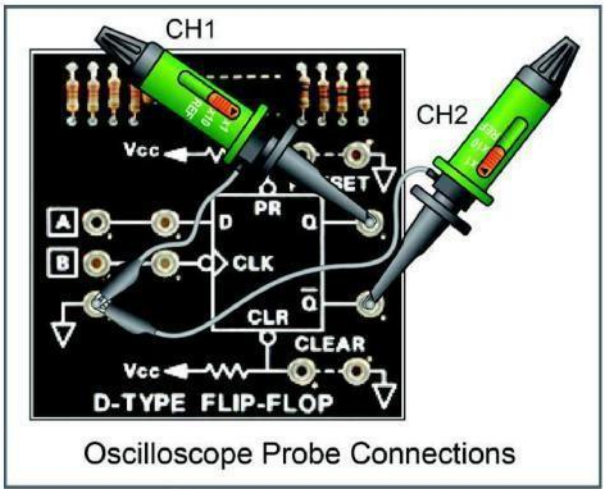
Modify your test circuit by connecting the CLK (clock) input of the D-TYPE FLIP-FLOP circuit block to the CLOCK circuit block. The CLK input is receiving a 50 kHz clock signal with a peak-to-peak amplitude of about 5 V. This means that there is a negative edge of the clock signal 50,000 times per second.



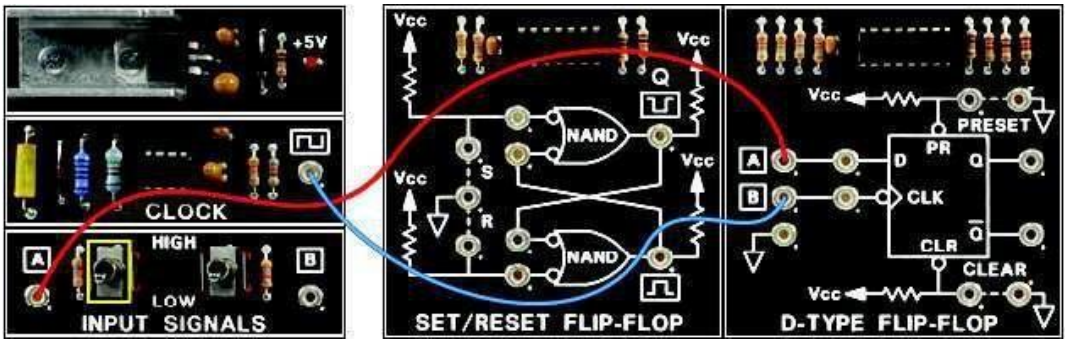
Q: Do the Q and Q! outputs change when the D input remains at logic 0?

a. yes b. no

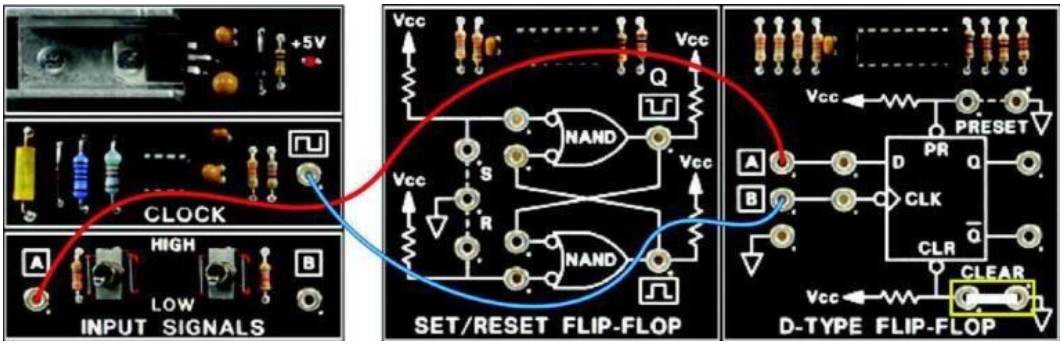




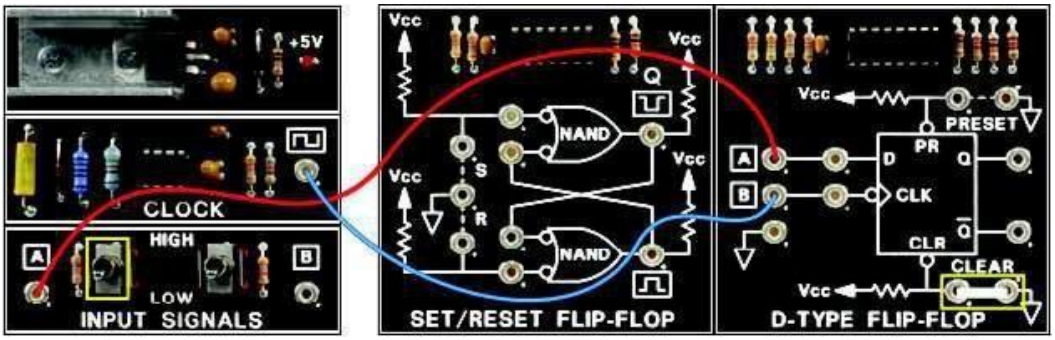
While observing the Q and Q! outputs on the oscilloscope screen, change the D input to logic 1 and back to logic 0 several times by changing the position of toggle switch A from LOW to HIGH and back to LOW several times.



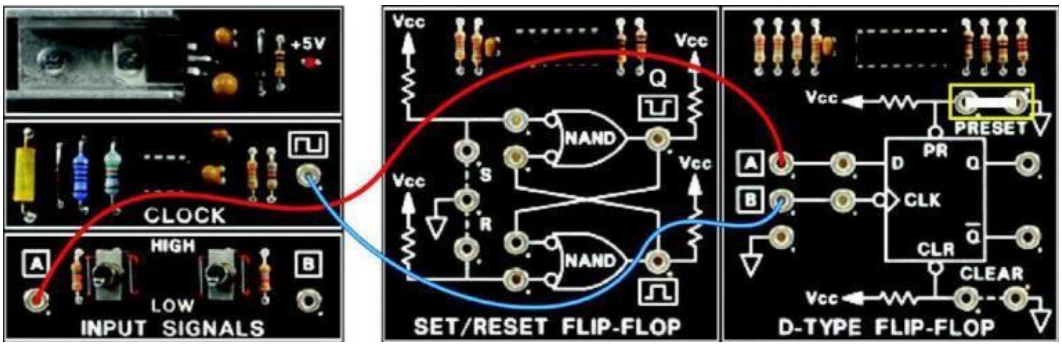
While observing the Q and Q! outputs on the oscilloscope screen, reset the CLR input to logic 0 by putting the two-post connector in the terminals at CLEAR.



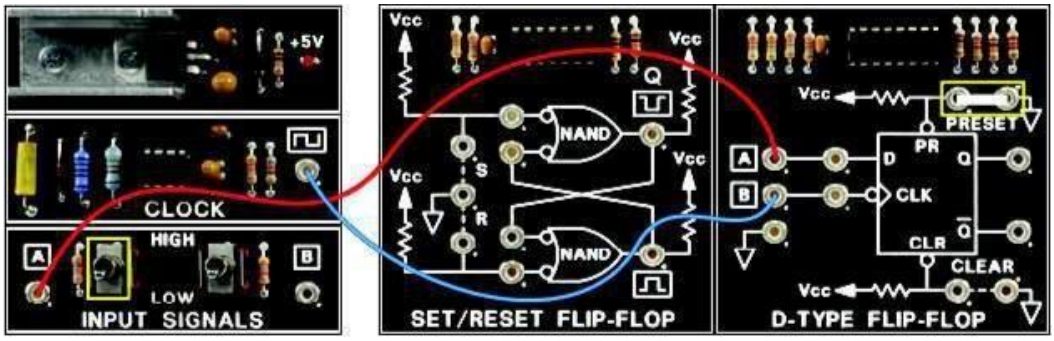
Move the toggle switch A to HIGH and back to LOW several times to change the logic state of D.



While observing the Q and Q! outputs of the oscilloscope screen, set the PR input by putting the two-post connector in the terminals at PRESET (remember that PR is active low).



Move the toggle switch A to HIGH and back to LOW several times to change the logic state of D.



Q: Based on your observation, does a logic 0 at the PR or CLR inputs initialize the logic state of the outputs?

a. yes b. no

➢ CONCLUSION

- A PR (preset) input sets the Q output to a logic 1 state.
- A CLR (clear) input resets the Q output to a logic 0 state.
- The two outputs, Q and Q!, are complementary.
- When PR and CLR are logic 1, Q equals the D input after the negative edge of the CLK signal.
- When PR and CLR are disabled, an input of 0 and 1 result with the RESET and SET states, respectively.
- The table shown describes the characteristics of the D-type flip-flop.

Inputs				Outputs	
Preset (PR)	Clear (CLR)	Clock (CLK)	Data (D)	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
1	1	1	X	Q	$\overline{Q}$
1	1	↓	1	1	0
1	1	↓	0	0	1
1	1	0	X	Q	$\overline{Q}$

X = Does not affect output

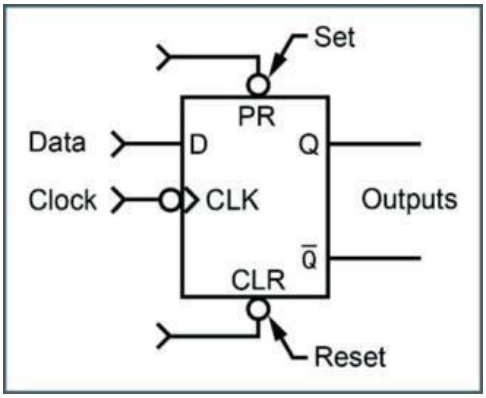
↓ = Negative clock transition (high-to-low) required

Q & $\overline{Q}$ = The level established from the last negative clock transition is maintained.

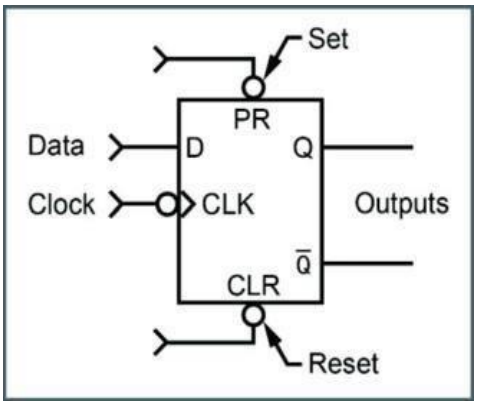
- **REVIEW QUESTIONS**

1. A D flip-flop
   a. immediately passes all input data (D) state changes to its output.
   b. does not react to input data (D) state changes until clocked.
   c. must be triggered with a negative clock edge to accept PR or CLR inputs.
   d. changes its output state at every negative clock edge.

2. A logic 0 at the PR (PRESET) input sets the Q output to logic
   a. 1. b. 0. c. 0 on a positive clock edge. d. 1 on a negative clock edge.



3. A logic 0 at the CLR (CLEAR) input resets the Q output to logic
   a. 1. b. 0. c. 0 on a positive clock edge. d. 1 on a negative clock edge.



4. In a D-type flip-flop:
    a. Q output follows the logic state of the D input.
    b. Q output follows the logic state of the CLK signal.
    c. outputs are both logic 0.
    d. outputs are locked in either the set or reset state, respectively.

LAB 5C: Synchronous Sequential Logic

➢ Objectives

- To learn the basic principles of latches and flip-flops which make up the basic building blocks of
  sequential logic circuits.

➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

➢ Background:

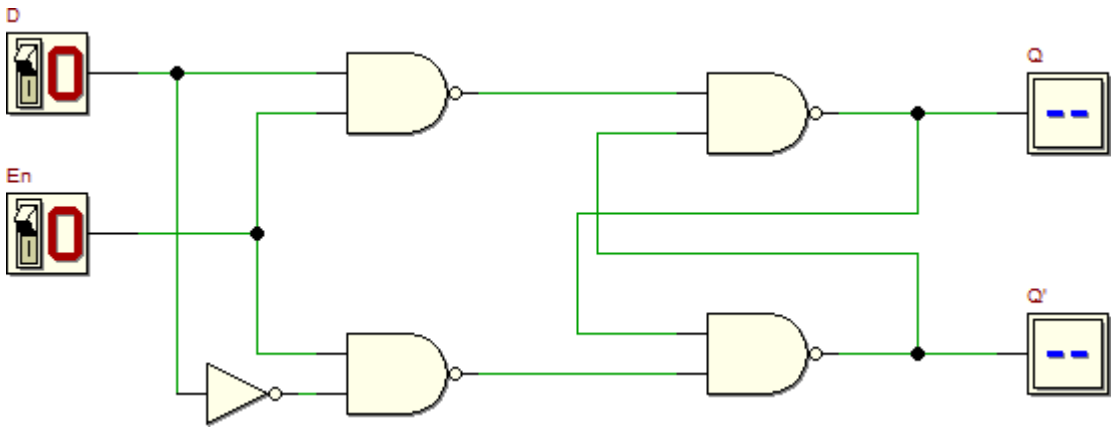
Try out the following exercises before your lab:
5.1, 5.4(a, b), 5.6, 5.7, 5.9 (a, b), and 5.10 (a, b, c)

➢ Simulation:

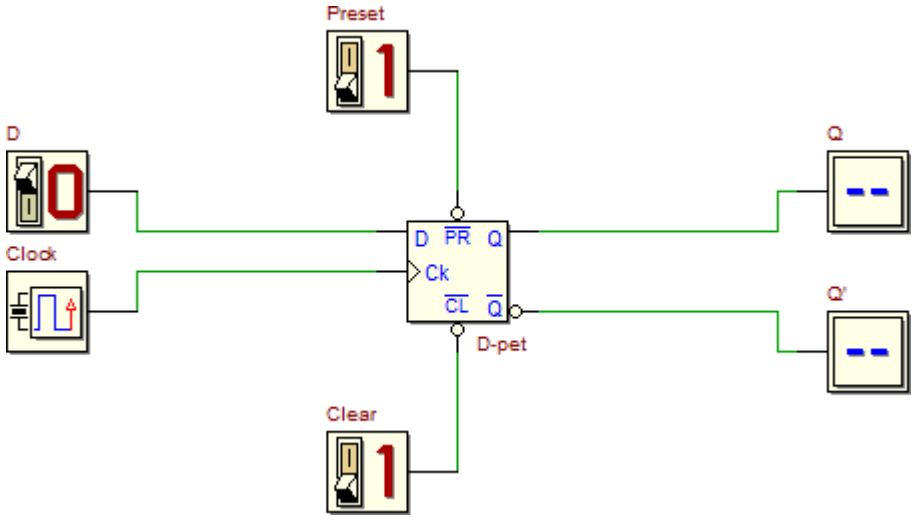
Simulate the following circuits. Write the State table for each flip-flop and Show the timing diagram for each.

a. D-Latch flip-flop
b. Positive edge-triggered D flip-flop
c. Positive edge-triggered J-K flip-flop.

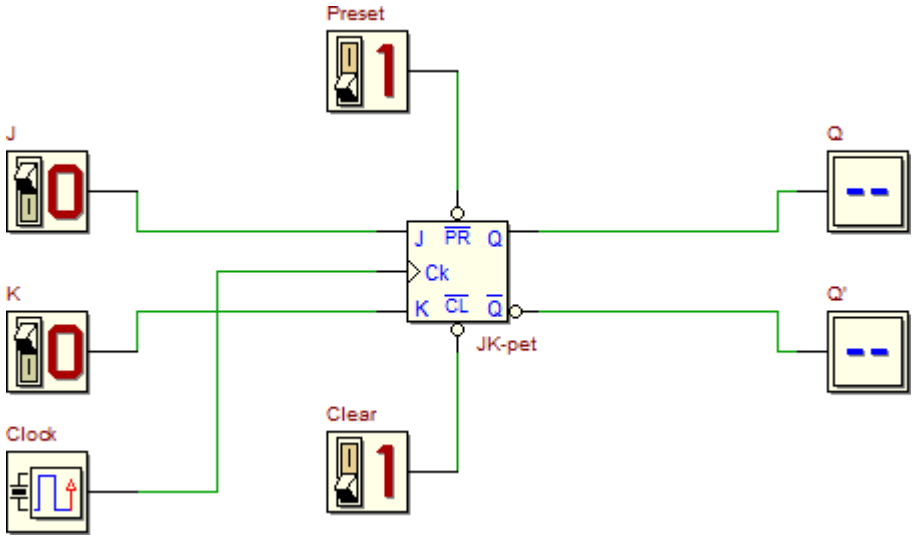
1- Use the simulator to draw each of the following sequential logic circuits in a separate file:



a) D-Latch flip-flop



b) Positive edg-triggered D flip-flop



c) Positive edge-triggered JK flip-flop

2- Start the **functional simulation (Interactive Animation)** of each flip-flop by clicking, on the **d-DcS toolbar**, the command  . Now the input switches of each circuit can be toggled and the corresponding outputs will be changed accordingly.

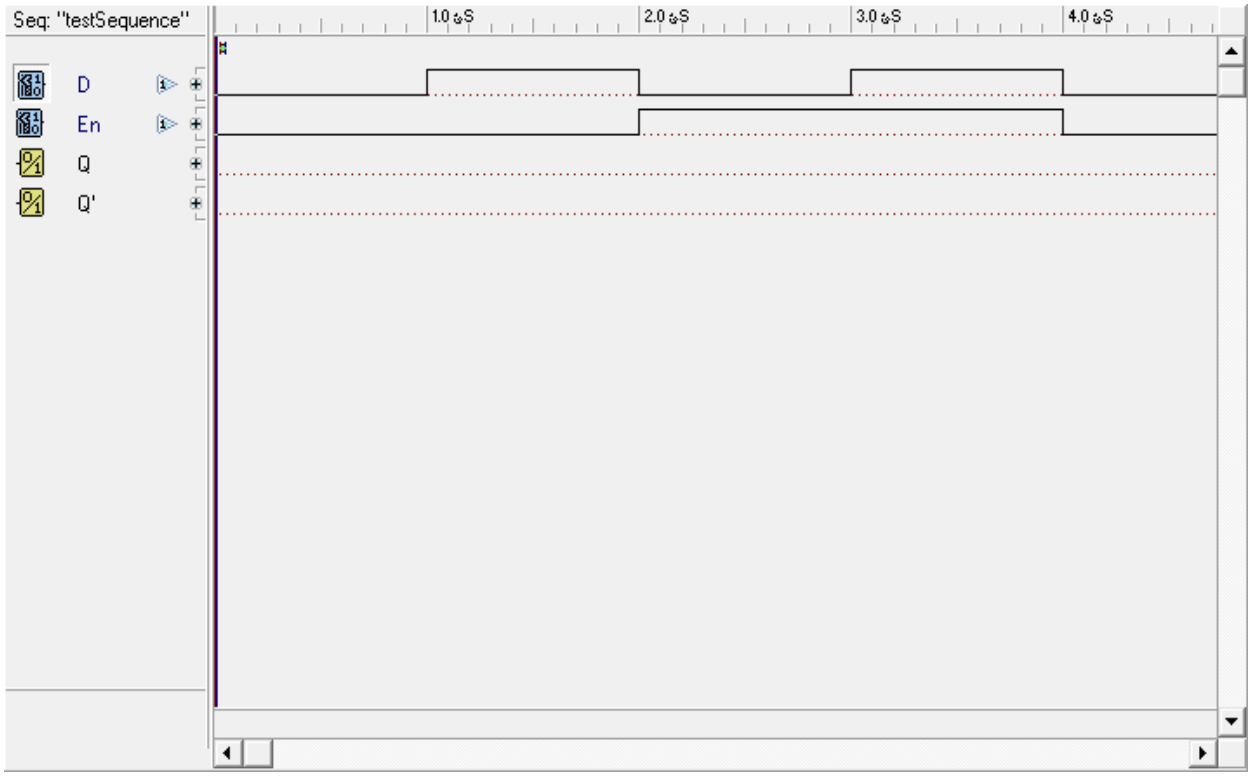
3- According to the simulation results of each flip-flop, fulfil the corresponding table of the following tables.

D-Latch flip-flop			
En	D	Q	Q'
0	0		
0	1		
1	0		
1	1		

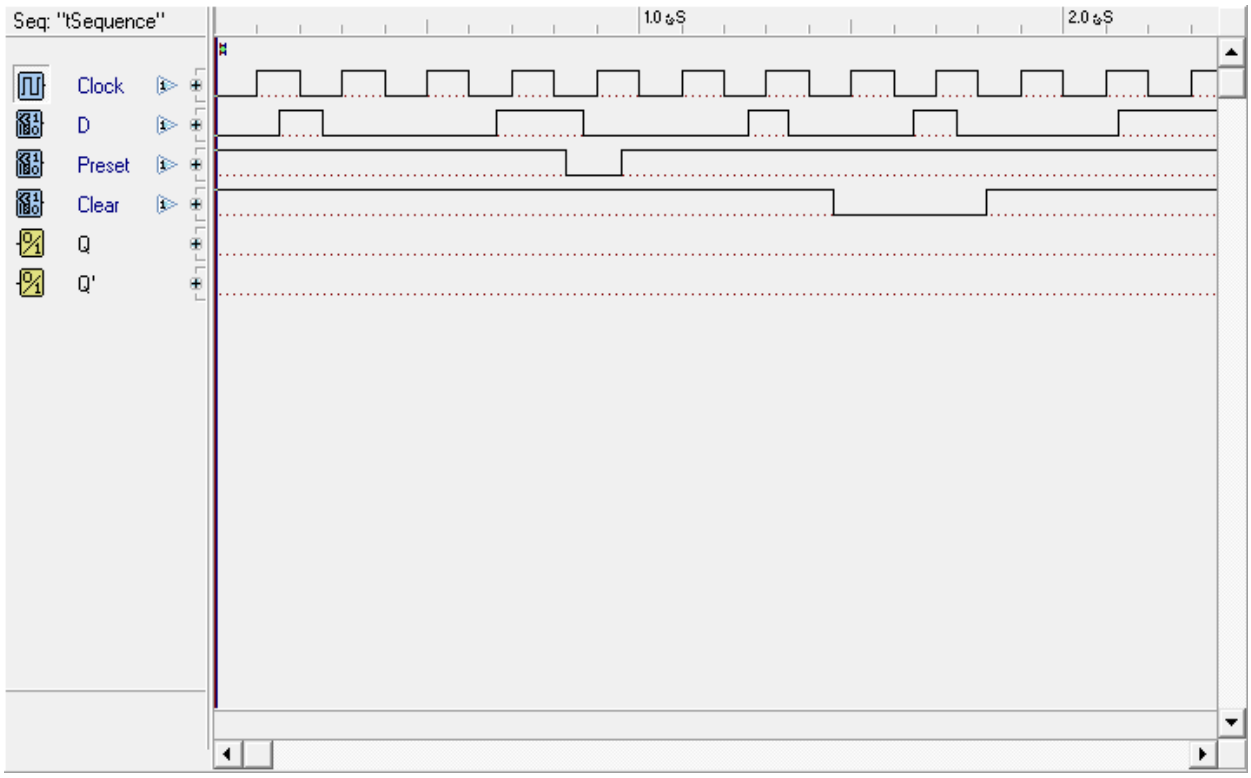
Positive edge-triggered D flip-flop					
D	Clock	Preset	Clear	Q	Q'
0	↑	1	1		
1	↑	1	1		
0	↑	0	0		
1	↑	0	0		

Positive edge-triggered JK flip-flop						
J	K	Clock	Preset	Clear	Q	Q'
0	0	↑	1	1		
0	1	↑	1	1		
1	0	↑	1	1		
1	1	↑	1	1		
0	0	↑	0	0		
0	1	↑	0	0		
1	0	↑	0	0		
1	1	↑	0	0		

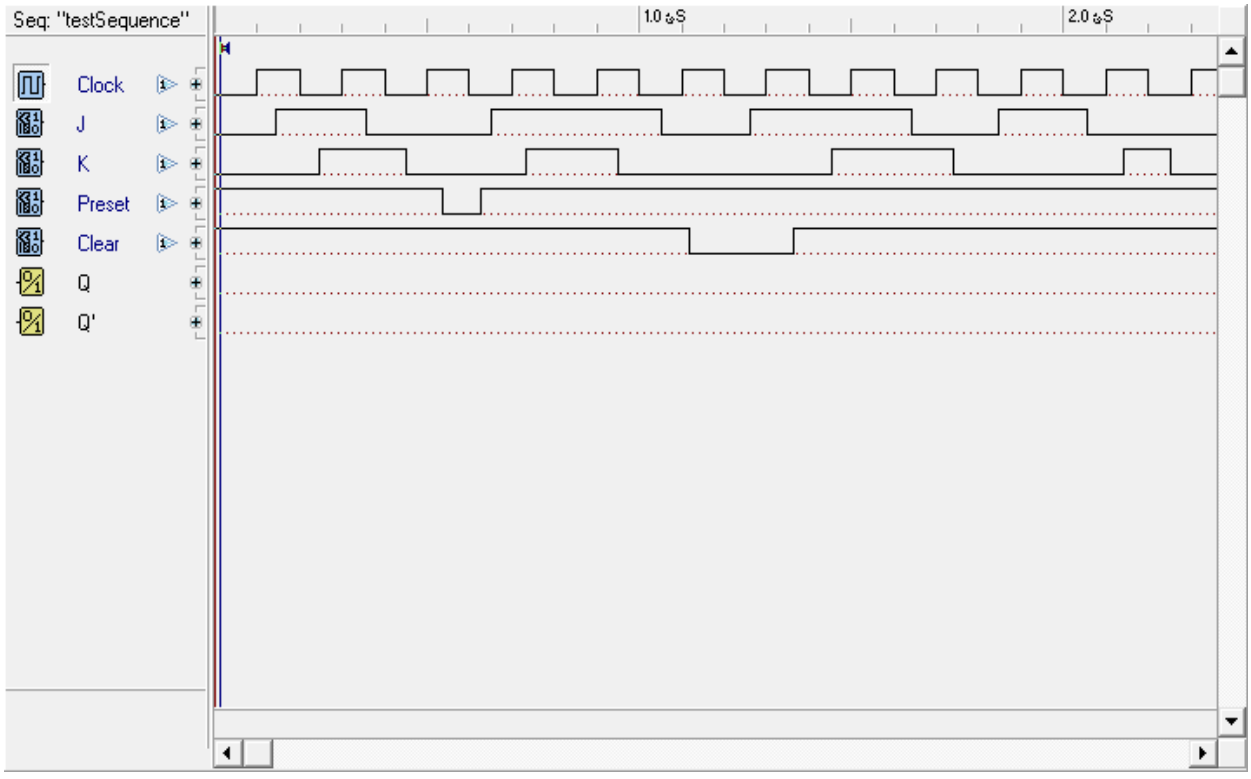
4- Check the **timing simulation** of each flip-flop by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window. You should define the values versus time of the inputs such as all the possible input combinations are tested. Also draw the output resulted from each **timing simulation** on the corresponding figure of the following figures.



a) D-Latch flip-flop timing diagram.



c) Positive edge triggered D flip-flop timing diagram.



c) Positive edge triggered JK flip-flop timing diagram.

- **Reflection Questions:** Student is required to submit the following:
  - Answers to the exercises **5.10 (a, b, c)** above.
  - Deadline: at the beginning of the next Lab session.

Student answer to the reflection question(if any)

LAB 5D: Sequential Circuit Analysis

➢ Objectives

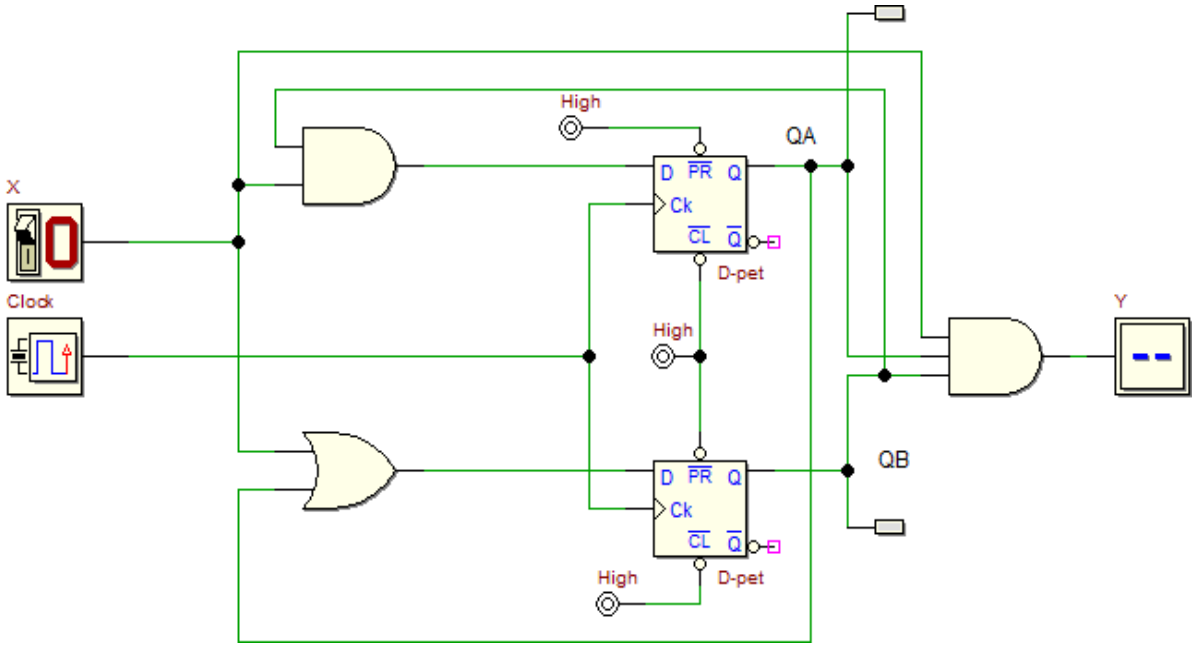
- To learn the basic principles of sequential circuit analysis.

➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

➢ Simulation:

1- Use the simulator to draw the following sequential logic circuits.

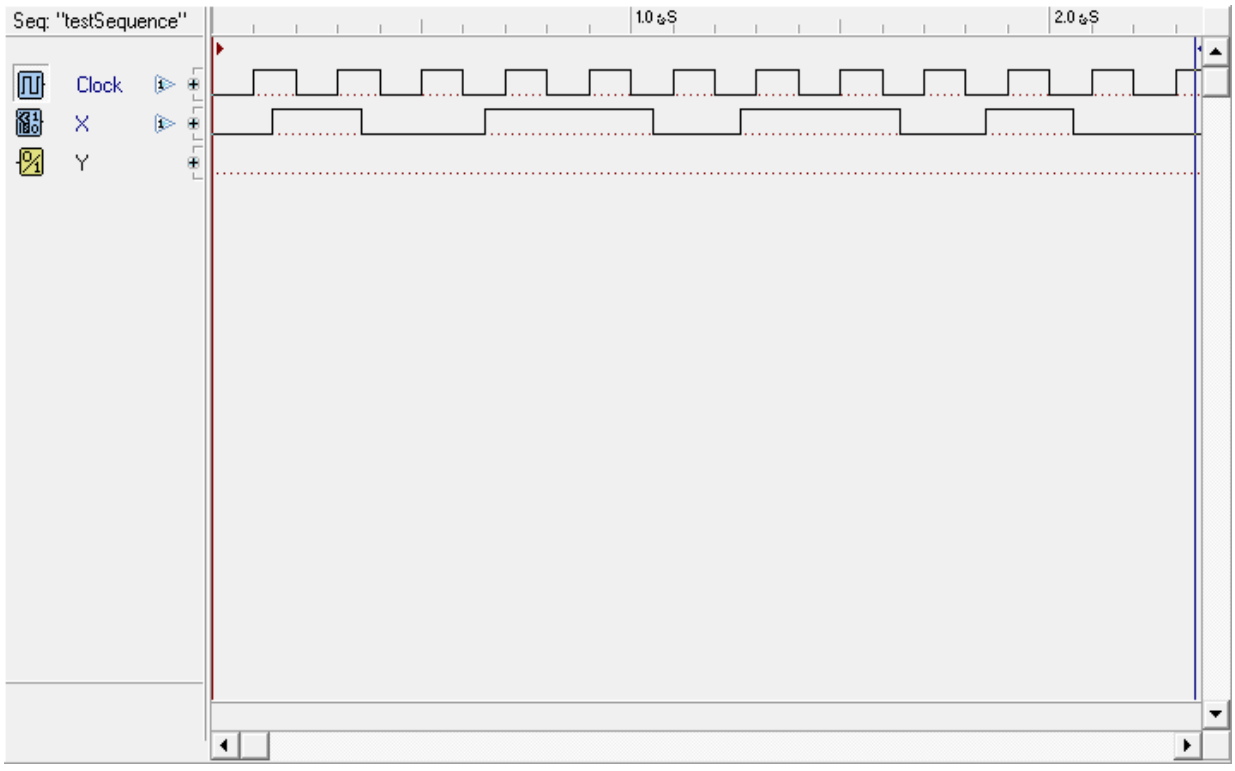


2- Start the **functional simulation (Interactive Animation)** of the sequential circuit by clicking, on the **d-DcS toolbar**, the command  . Now the input switch of the circuit can be toggled and the corresponding outputs will be changed accordingly.

3- According to the simulation results, fulfil the following state table.

Present-state		Input	Next-state		Output
QA	QB	X	QA	QB	Y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

4- Check the **timing simulation** of the given sequential circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window as shown in the following figure. Each student is required to draw the output resulted from the **timing simulation** on the figure below.



Lab 6A: Registers

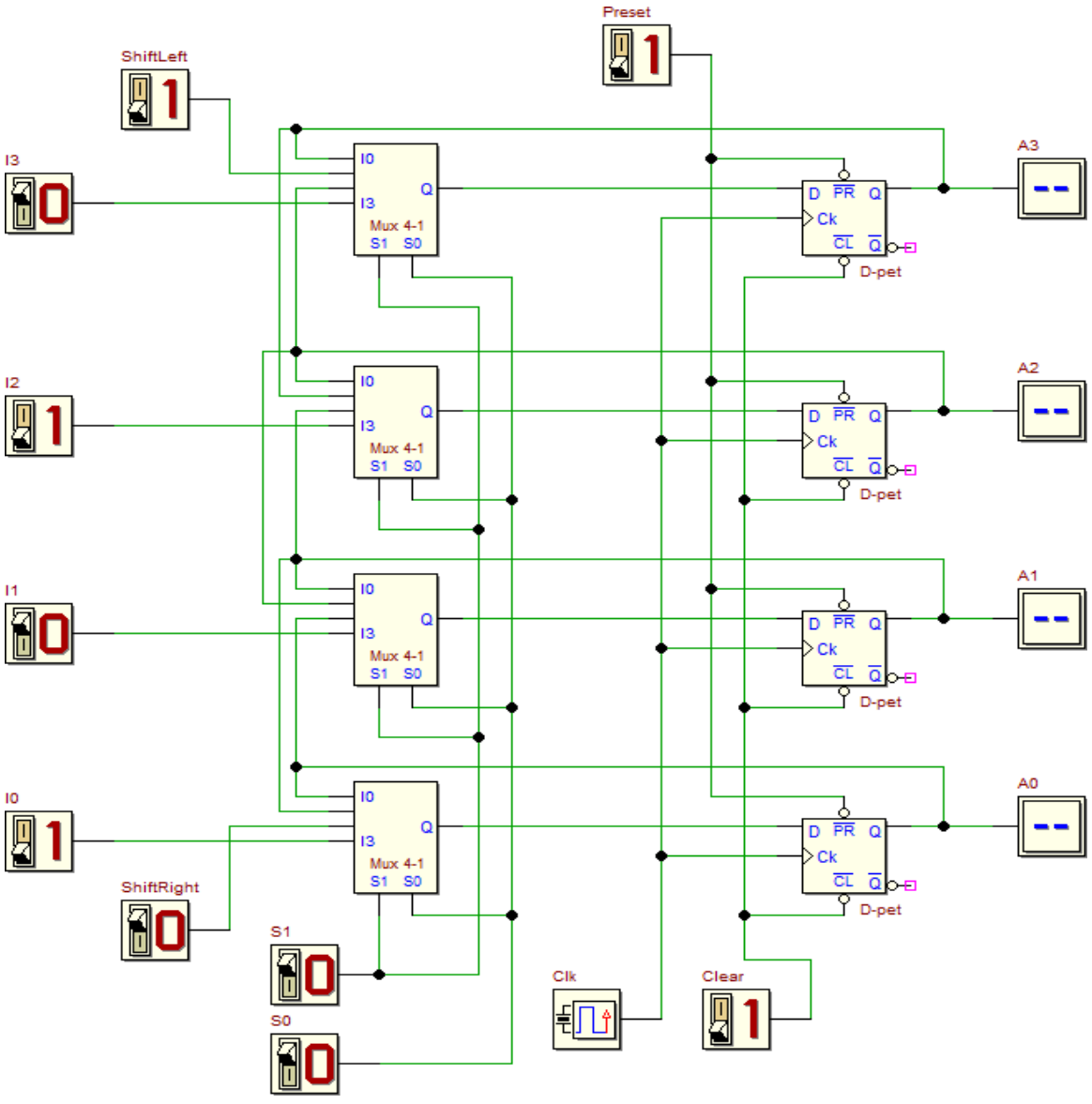
- **Objectives**
  - To learn the different types of registers such as parallel load registers and shift registers.

- **Requirements:**
  - A desktop or laptop computer.
  - Download the Deeds (Digital Electronics Education and Design Suite) software.

- **Background:** Try out the following exercises before your lab.
  6.3, 6.4, 6.6, and 6.7

- **Simulation:**
  Simulate the Four-bit universal shift register shown in the figure below. Show the **timing diagram** and Write its function table.

  1- Use the simulator to draw the following sequential logic circuits with the specified initial input values.

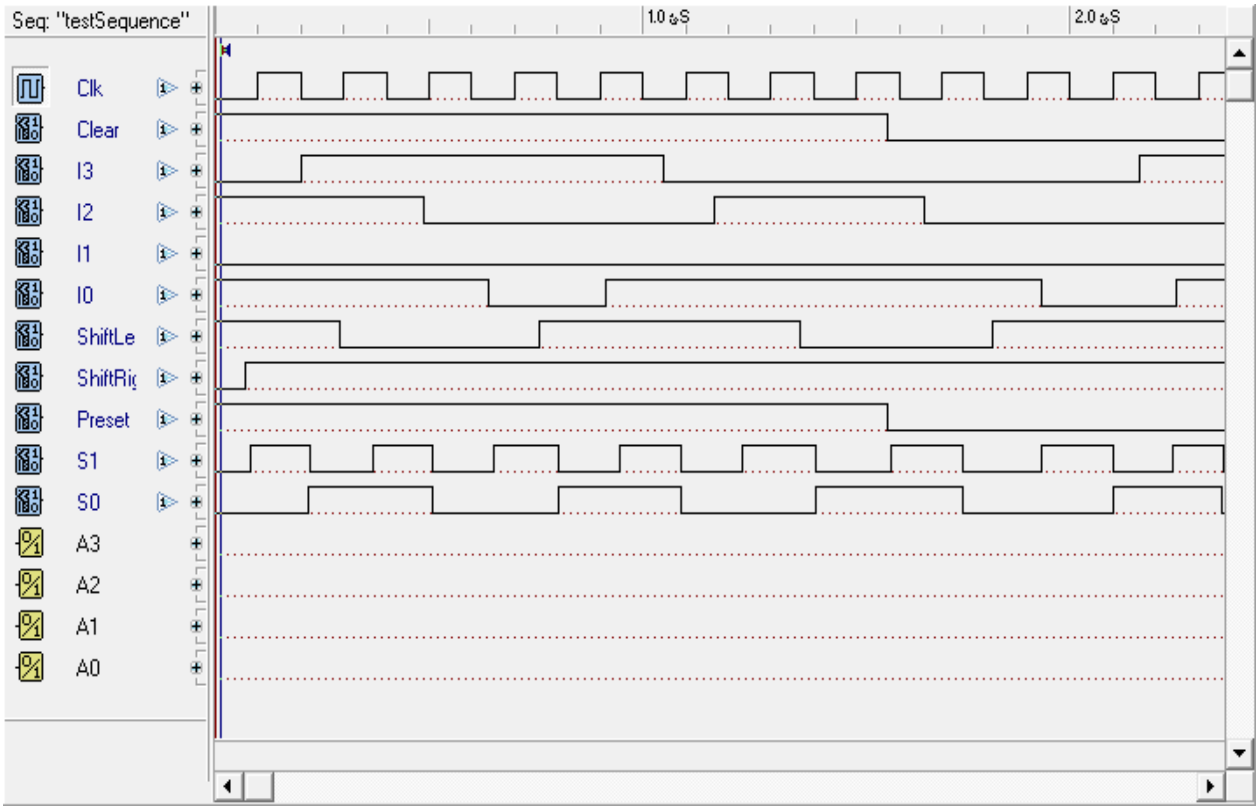


2- Start the **functional simulation (Interactive Animation)** of the sequential circuit by clicking, on the **d-DcS toolbar**, the command  . Now switch the inputs to their initial values and change only the selection switches.

3- After four clock cycles for each operation (i.e., selection mode), complete the following table .

Positive edge-triggered JK flip-flop									
S1	So	Clock	Preset	Clear	A3	A2	A1	A0	Register Operation
0	0	↑	1	1					
0	1	↑	1	1					
1	0	↑	1	1					
1	1	↑	1	1					
0	0	↑	0	0					
0	1	↑	0	0					
1	0	↑	0	0					
1	1	↑	0	0					

4- Check the **timing simulation** of the universal shift register by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window as shown in the following figure. Each student is required to draw the output resulted from the **timing simulation** on the figure below.



- **Reflection Question**:

  Student is required to submit the following:
  - Answers to the exercises 6.6 and 6.7 above.
  - Deadline: The beginning of the next Lab session.

Student answer to the reflection questions:

Lab 6B: Synchronous Counter

- **OBJECTIVE**

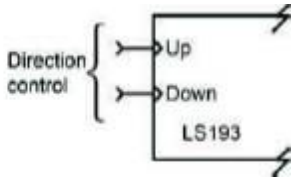
When you have completed this exercise, you will be able to describe the waveforms associated with a synchronous counter. You will verify your results by observing the waveforms on your oscilloscope.

- **REQUIREMENTS**
  - DIGITAL CIRCUIT FUNDAMENTALS (LabVolt) Circuit Board
  - PC or a Laptop computer
  - An oscilloscope

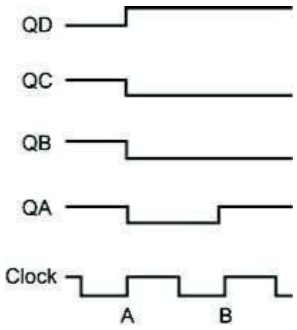
- **DISCUSSION**

The LS193 synchronous counter has two input signals (UP and DOWN) associated with clocking and count direction. The signal conditions required at the UP and DOWN inputs to control your counter are given in the table.

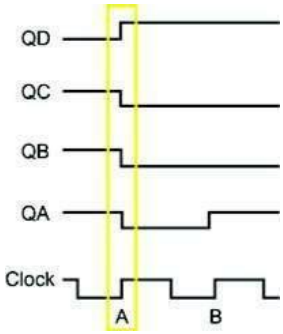
Up Input	Down Iinput	Result
Pulsed	High	Up count
High	Pulsed	Down count



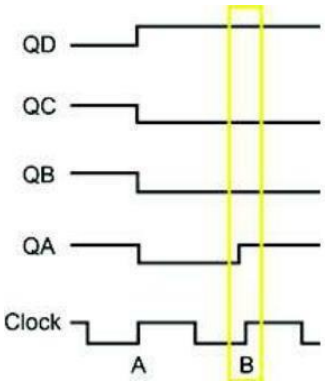
An advantage of the synchronous counter over the asynchronous type is that all outputs can be clocked simultaneously.



All the outputs change simultaneously at clock A time.



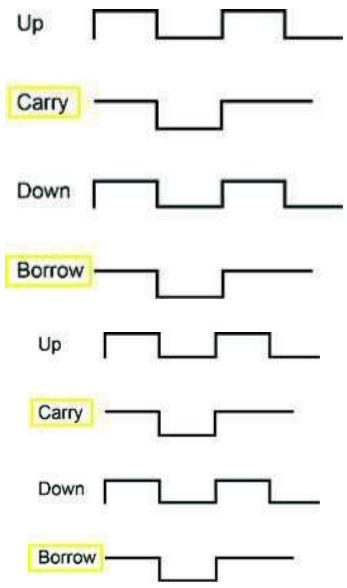
At clock B time, only QA changes. This indicates that only QA required an update.



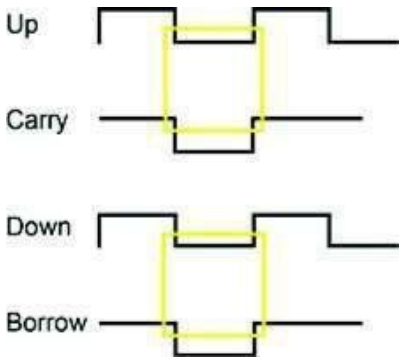
Although a synchronous counter can update all outputs simultaneously, the outputs that actually change are a function of the count value. This concept is illustrated below.

QD	QC	QB	QA	BITS changed
1	0	0	0	All changed
0	1	1	1	
0	1	1	0	Only QA changed
0	1	0	1	QB/QA changed

The internal gates of your counter generate CARRY and BORROW output pulses. Each pulse occurs at the same time as the circuit CLOCK input.

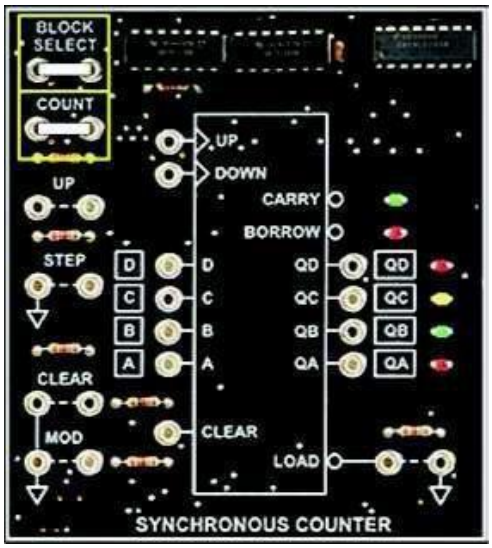


On your circuit, the pulse width of the CARRY and BORROW outputs equals the pulse width of the UP or DOWN input.



- **PROCEDURE**

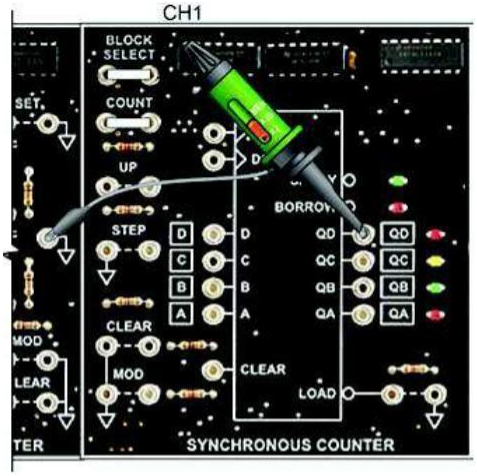
Locate the SYNCHRONOUS COUNTER circuit block, and connect the circuit shown.
NOTE: Your counter should be in a free-run, or count, mode.

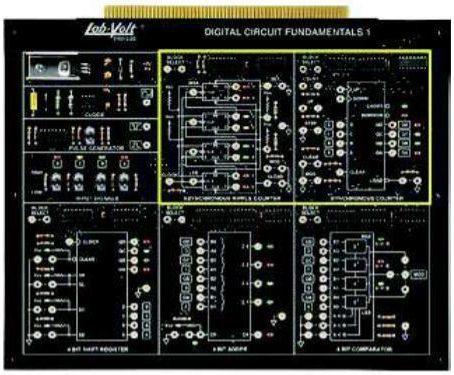


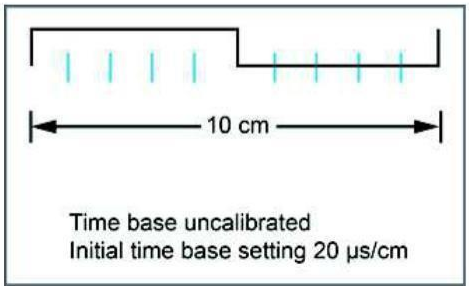
Connect channel 1 of your oscilloscope to the QD output of your circuit. Synchronize your oscilloscope on QD.

Set the time base on your oscilloscope to 20. One complete cycle of the QD waveform occupies exactly 10 cm (10 horizontal boxes on the oscilloscope grid).

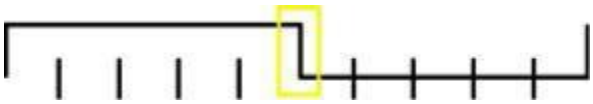
NOTE: Do not alter the oscilloscope time base settings.







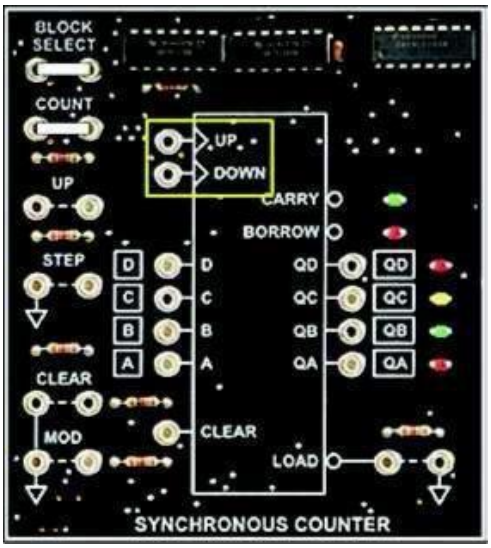
Use channel 2 of your oscilloscope to monitor, in turn, the DOWN, QC, QB, and QA circuit waveforms. Observe each waveform at the time that QD, your reference waveform, undergoes a positive to negative transition (midpoint of QD waveform).



Q: Do the output waveforms change synchronously with the circuit clock (input at the DOWN terminal)?

a. yes b. no

Use channel 2 of your oscilloscope to determine which circuit CLOCK input is active.



Q: Based on your observations, the counter

a. decrements. b. increments.

Enable the UP function of your circuit.

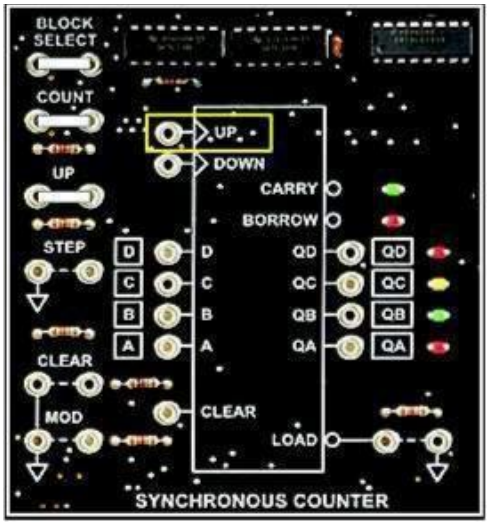
Q: Which signal conditions are established for the UP and DOWN circuit inputs?

a. Both inputs are pulsed. b. UP is high, and DOWN is pulsed.

c. UP is pulsed, and DOWN is high. d. Both inputs are static.

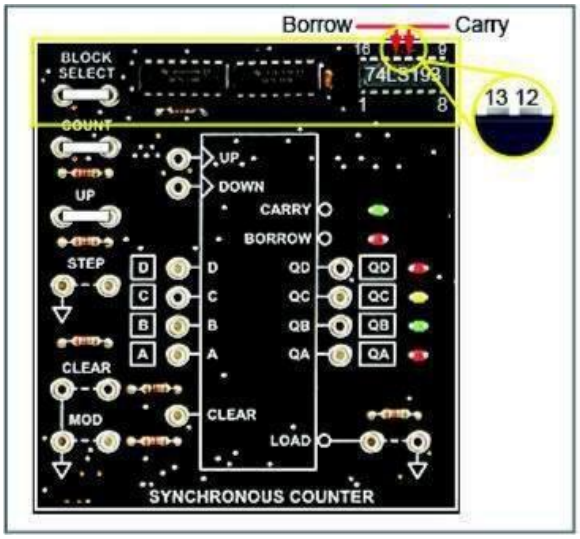
Place CM switch 5 in the ON position to lower the clock frequency of your counter.

Place CM switch 5 in the OFF position. Adjust the TIME VARIABLE control of your oscilloscope to its calibrated position. Move channel 1 of your oscilloscope to the circuit CLOCK input (UP terminal of the IC).



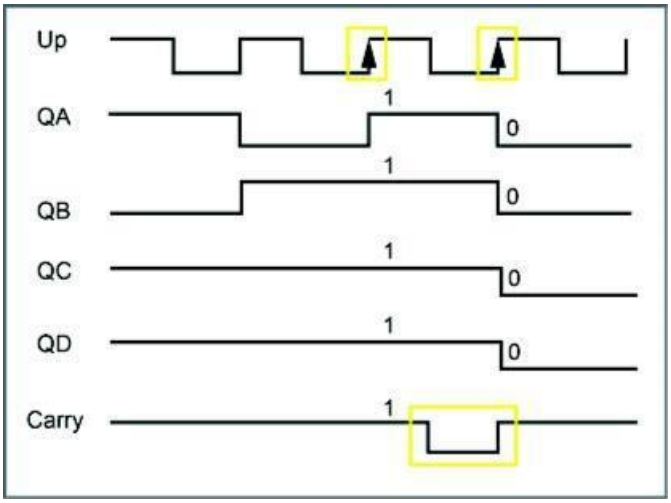
Use channel 2 of your oscilloscope to carefully measure the CARRY pulse directly at pin 12 of the LS193 chip.

NOTE: Synchronize your oscilloscope on the negative edge of the channel 2 waveform.

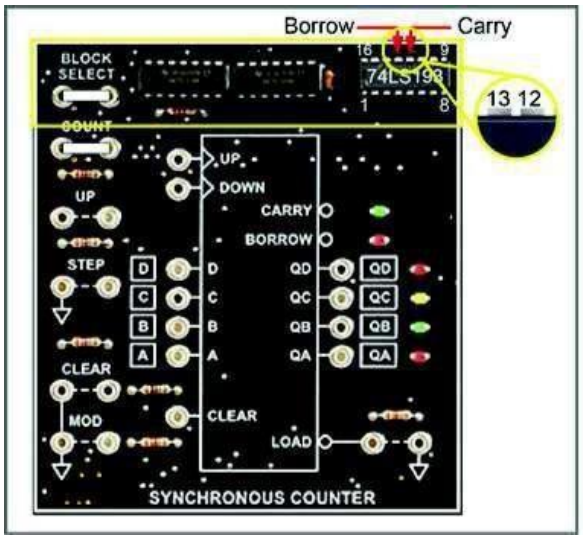


Q: What is the pulse width relationship between the CLOCK and CARRY waveforms?

a. The CARRY signal pulse width is greater than that of the CLOCK signal.
b. The CARRY pulse width equals that of the negative phase of the clock.
c. The CARRY signal pulse width is less than that of the CLOCK signal.



Select the DOWN function of your counter. Use channel 2 of your oscilloscope to carefully measure the BORROW pulse directly at pin 13 of the LS193 IC chip.
NOTE: Move channel 1 to the DOWN terminal of the IC, and synchronize your oscilloscope on the negative edge of the channel 2 waveform.



Q: What is the pulse width relationship between the CLOCK and BORROW waveforms?

a. The BORROW signal pulse width is greater than that of the CLOCK signal.
b. The BORROW pulse width equals that of the negative phase of the clock.
c. The BORROW signal pulse width is less than that of the CLOCK signal.

Make sure all CMs are cleared (turned off) before proceeding to the next section.

➢ CONCLUSION

- The outputs of a synchronous counter are clocked simultaneously.
- On the 74LS193 counter, the UP and DOWN inputs comprise the chip CLOCK input.
- If UP is held high as DOWN is pulsed, the counter decrements.
- If DOWN is held high as UP is pulsed, the counter increments.
- The pulse width of CARRY and BORROW equals the pulse width of the negative phase of the CLOCK.

➢ REVIEW QUESTIONS

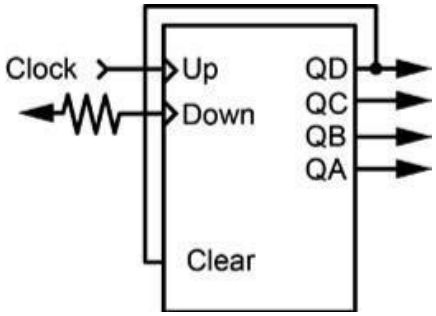
1. The outputs of a synchronous counter
   a. must all change at once for every CLOCK input.
   b. will change simultaneously.
   c. can increment and decrement simultaneously.
   d. can produce simultaneous CLEAR and BORROW indications.

2. To clock the LS193, the CLOCK inputs
   a. must both be pulsed.
   b. must both be held high.
   c. require complementary square wave inputs.
   d. require a high level on one input and a pulsed level at the other input.

3. A CARRY output is generated
   a. as the count value increments from 1111 to 0000.
   b. as the count value increments from 1110 to 1111.
   c. once on the way up and again on the way down.
   d. None of the above

4. A BORROW output is generated
   a. as the count value decrements from 0000 to 1111.
   b. as the count value decrements from 1111 to 1110.
   c. once on the way down and again on the way up.
   d. None of the above

5. On this counter circuit, the QD feedback
   a. has no effect on circuit operation.
   b. locks the counter into a constant reset state.
   c. forces the counter to decrement.
   d. forces a maximum count indication of 7.



Lab 6C: Counters

➢ Objectives

- To learn the different types of counters such as asynchronous/synchronous and up/down counter, how to design synchronous counters, and counter decoding.
- You are required to work individually and answer the following questions.

➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

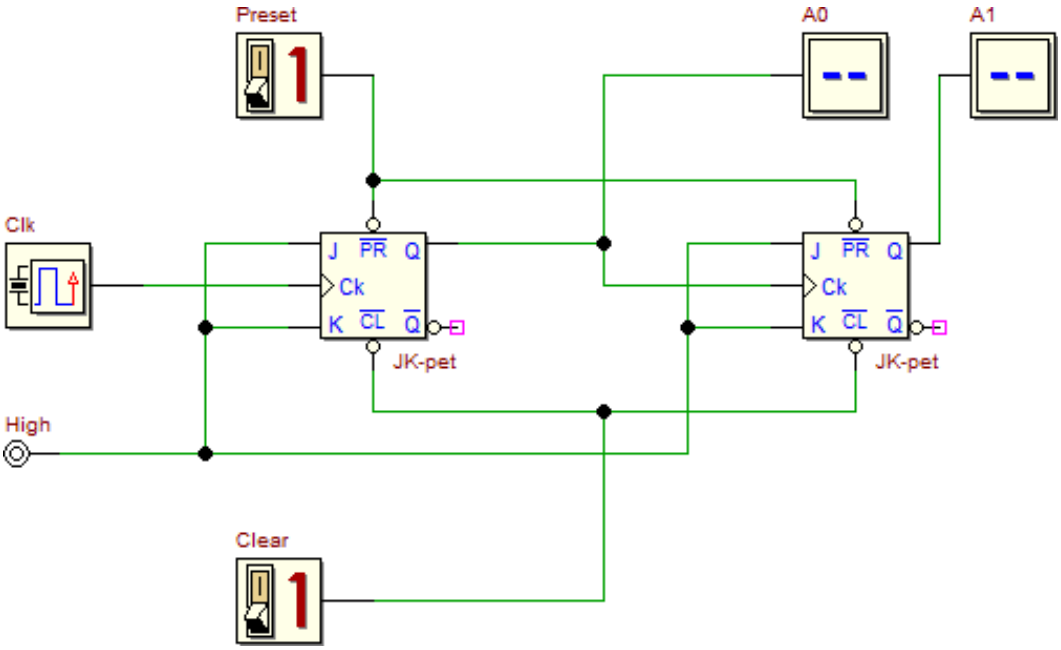
➢ Background:

Try out the following exercises before your lab.
6.11, 6.13, 6.17, 6.24, 6.27

➢ Simulation:

Simulate the following **Two-bit binary ripple counter** circuits. Show the **timing diagram**.

1- Use the simulator to draw the following sequential logic circuits with setting the values of *Preset* and *Clear* switches to 1's as shown in the figure below.



2- Start the **functional simulation (Interactive Animation)** of the sequential circuit by clicking, on the **d-DcS toolbar**, the command  . Then switch the *Clear* switch from 1 to 0 and return it back to 1. Observer the outputs and discuss the results.

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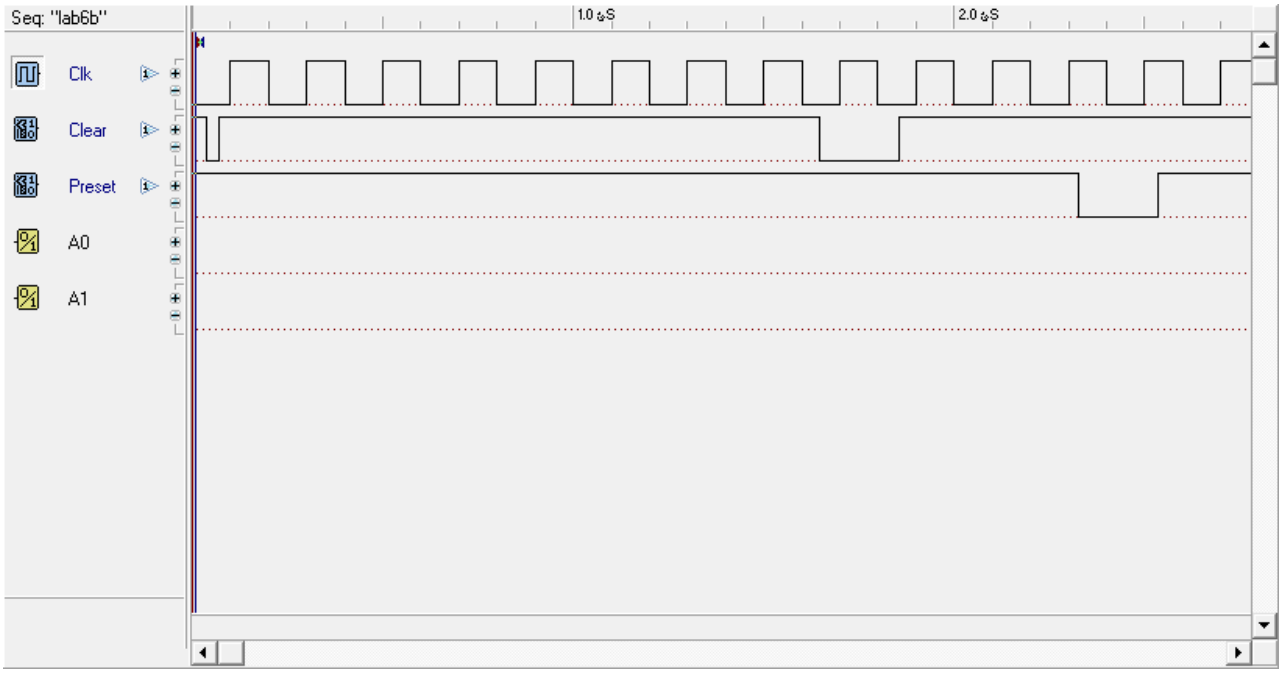
4- Check the **timing simulation** of the given sequential circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window as shown in the following figure. Each student is required to draw the outputs **A0** and **A1** resulted from the **timing simulation** on the figure below.



Reflection Question: Student is required to submit the following:

- Answers to the exercises 6.11 and 6.13 above.
- Deadline: The beginning of the next Lab session.

Student answer to the reflection question (if any)

Lab 6D: Counters and Decoders

➢ Objectives

- To learn how to use counters with decoders

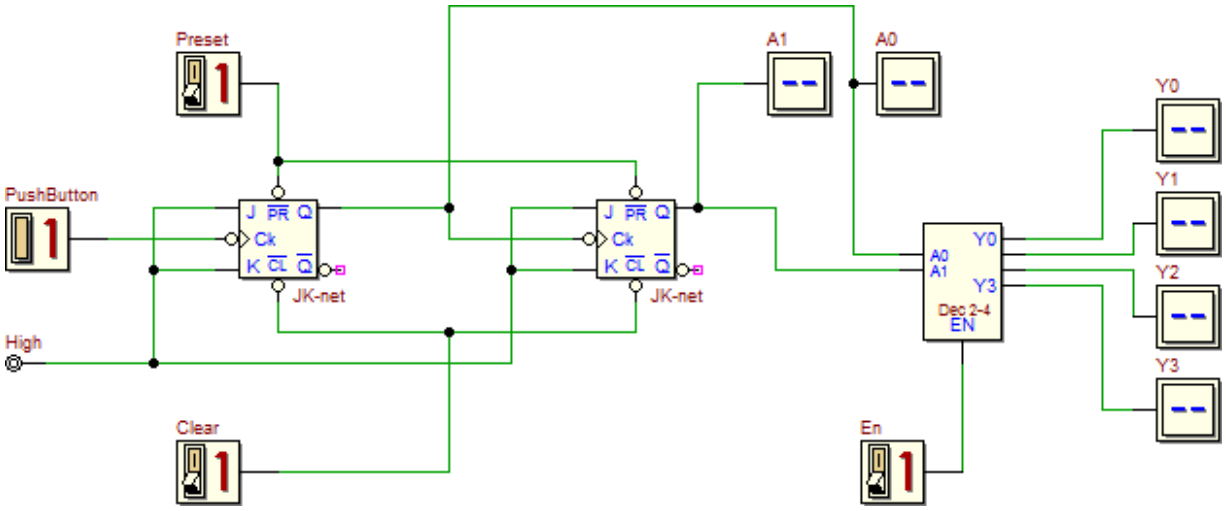
➢ Requirements:

- A desktop or laptop computer.
- Download the Deeds (Digital Electronics Education and Design Suite) software.

➢ Simulation:

Simulate the 2-bit counter with a 2-t0-4 decoder and show the **timing diagram.**.

1- Use the simulator to draw the following circuit with the specified initial values of the switches.



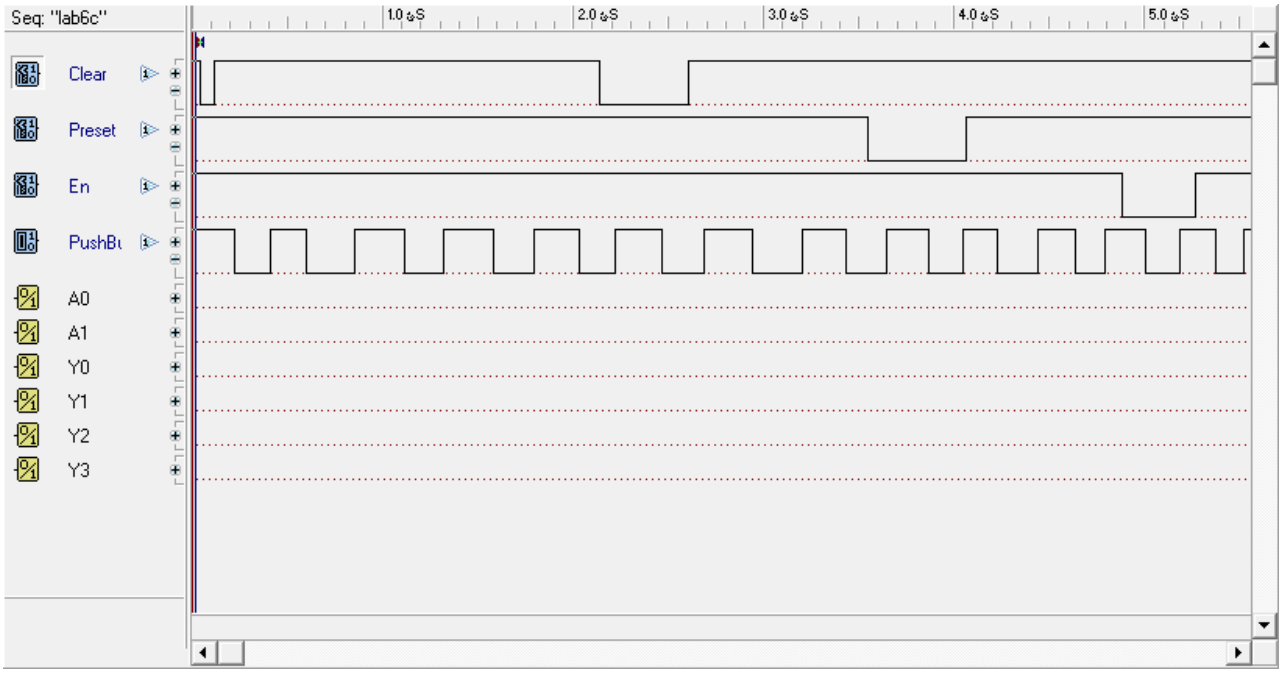
2- Start the **functional simulation (Interactive Animation)** of the sequential circuit by clicking, on the **d-DcS toolbar**, the command  .

3- Switch the *Clear* switch from 1 to 0 and then return it to 1.

4- Push on the button " PushButton" ten times and record the results in the following table.

PushButton	Clear	En	A0	A1	Y0	Y1	Y2	Y3
1	1	1						
2	1	1						
3	1	1						
4	1	1						
5	1	1						
6	1	0						
7	1	0						
8	0	0						
9	0	0						
10	0	0						

4- Check the **timing simulation** of the underlying circuit by clicking, on the **d-DcS toolbar**, the command  . The input values must be drawn directly on the timing diagram window as shown in the following figure. Each student is required to draw the output resulted from the **timing simulation** on the figure below.



5- Write here what you have leant from this experiment.

LAB 7: Memory and Programmable Logic

➢ Objectives

- To learn the basics behind the memory and programmable logic through a set of problems.

➢ Background:

Try out the following exercises before your lab.
7.1, 7.9, 7.14, 7.15, 7.22, 7.25, 7.28

During the lab, the TA will answer the exercises 7.1, 7.9, 7.14, and 7.15**.**

➢ Reflection Questions:

Student is required to submit the following:

- Answers to the exercises 7.22, 7.25 and 7.28 above.
- Deadline: Before the final lab test.

Student answer to the reflection questions:

References

[1] LabVolt Courseware and LMS material, https://www.labvolt.com/courseware_platforms.